Course Outline (F2023)

COE758: Digital Systems Engineering

Instructor(s)	Dr. Vadim Geurkov [Coordinator] Office: ENG430 Phone: (416) 979-5000 x 556088 Email: vgeurkov@torontomu.ca Office Hours: TBD
Calendar Description	The emphasis of this course is an understanding of the system architecture around the processor. Course covers all types of modern semiconductor memory, cache and virtual memory organization, hard disk drives and video-output subsystem. Course gives classification of buses and description of concepts of bus organization, bus protocols, arbitration mechanisms and the concept of Direct Memory Access (DMA). The laboratory projects include design of Cache Controller and VGA-signal generator using VHDL in Xilinx CAD environment.
Prerequisites	(COE 538 or ELE 538) and COE 608
Antirequisites	None
Corerequisites	None
Compulsory Text(s):	1. David Patterson and John Hennessy, "Computer Organization and Design: The hardware/Software Interface", 5-th edition, Morgan Kaufman Publishers Inc., San Francisco, CA USA, ISBN-9780124077263 2. Marilyn Wolf, "Computers as Components: Principles of Embedded Computing System Design", Fourth Edition, Morgan Kaufmann is an imprint of Elsevier, Cambridge, MA 02139, United States USA, ISBN: 978-0-12-805387-4 3. Vincent Heuring and Harry Jordan, "Computer Systems Design and Architecture", Second edition, Prentice Hall, Pearson Education Inc., NJ, 07458, ISBN 0-13-048440-7
Reference Text(s):	1. https://www.ee.ryerson.ca/~lkirisch/coe758/handouts.htm
Learning Objectives (Indicators)	At the end of this course, the successful student will be able to: 1. Understand the concepts of memory hierarchy organization and be able to apply this knowledge for the design of major architectural components of modern computer systems: cache memory, cache and main memory controllers, virtual memory elements and associated hardware/software drivers. Describe principles of interfacing the processor with different types of Input / Output (I/O) devices, estimate bus bandwidth, select the most effective bus organization and design I/O device controllers & adapters for modern computer systems. (**4a**) 2. Describe principles of interfacing the processor with different types of Input / Output (I/O) devices, estimate bus bandwidth, select the most effective bus organization and design I/O device controllers & adapters for modern computer systems. Learn modern integrated CAD tools (e.g. Xilinx ISE) and Hardware Description Languages (e.g. VHDL) and apply the principles of on-chip hardware design: including symbol creation, top-bottom design, high-

level synthesis of IP-core architecture for designing the on-chip (FPGA-based) IP-cores for cache controllers, main memory interfaces, I/O device controllers and interfaces to real-time peripheral devices. (**4b**)
3. Integrate the on-chip (FPGA-based) IP-cores with the host computer and real-time peripheral device (e.g. SVGA video-display) and adjust timing parameters of the designed on-chip device controller. (**4c**)
4. Utilize the on-chip debugging techniques for modern FPGA-based hardware platforms (e.g. Xilinx Spartan FPGA devices), including synthesis and application of the on-chip test-vector generators, utilization of on-chip logic analyzers (e.g. Xilinx ChipScope), creation of the hardware emulation environment and systematic analysis of timing diagrams received from the on-chip logic analyzers. (**5a**)
5. Produce project reports using appropriate format of technical reports, grammar, and citation styles for technical and non-technical audiences. (**7a**)
6. Illustrate concepts including the structure of IP-cores VHDL-code with appropriate comments and obtained experimental results. (**7c**)

NOTE: *Numbers in parentheses refer to the graduate attributes required by the Canadian Engineering Accreditation Board (CEAB).*

Course Organization	3.0 hours of lecture per week for 13 weeks 2.0 hours of lab per week for 12 weeks 0.0 hours of tutorial per week for 12 weeks
Teaching Assistants	TBA

Course Evaluation

Theory	
Midterm Exam	25 %
Final Exam	45 %
Laboratory	
Tutorials	2 %
Lab Project 1	14 %
Lab Project 2	14 %
TOTAL:	100 %

Note: In order for a student to pass a course, a minimum overall course mark of 50% must be obtained. In addition, for courses that have both **"Theory and Laboratory"** components, the student must pass the Laboratory and Theory portions separately by achieving a minimum of 50% in the combined Laboratory components and 50% in the combined Theory components. Please refer to the **"Course Evaluation"** section above for details on the Theory and Laboratory components (if applicable).

Examinations	Midterm exam in Week 7, two hours, closed book, problem solving (covers Weeks 1-6). Final exam, three hours, closed-book, problem solving (covers all course material).
Other Evaluation Information	The laboratory projects include design of IP-cores of custom on-chip modules for cache controller and video-signal generator for SVGA-monitor. Both projects include all major stages of on-chip design of custom digital systems: coding on VHDL hardware description language, compilation and design evaluation in Xilinx ISE CAD environment and hardware implementation on Xilinx Spartan FPGA platform.

In assigned projects, students are required to develop the custom IP-cores on the basis of Xilinx Spartan FPGA development platform. The goal is to apply the theoretical knowledge to on-chip system design and get practical experience in VHDL-coding, simulation and on-chip verification of the designed module.

There are two projects associated with different aspects of the system-on-chip (SoC) design:
1) IP-core design of the control-dominated circuit (Project 1: Cache Controller) and
2) IP-core design of the data-path dominated circuit (Project 2: Video-signal generator).

For both projects the requirements are to demonstrate ability to create symbol of the system, develop system block-diagram, write the VHDL-code, compile and simulate it in Xilinx CAD environment, verify the behaviour on the Xilinx Spartan FPGA development platform using on-chip instrumentation (Chip-Scope), demonstrate the complete IP-core performance and submit the project report.

Additionally, Project 2 requires integration the FPGA platform with the real-time I/O device (SVGA video-monitor) and demonstrate working project in all modes of operation.

Lab Management

The completed Tutorials account to 2% and lab Projects account for 14% each of the final mark. Each project must be demonstrated during the demonstration week. The project report must be submitted after successful project demonstration before the end of the demonstration week.
The detailed evaluation of Lab components and projects is as follows:
  1. 2% - Completed tutorials
  2. 14% for each project:
     2% - Symbol & block diagram design
     3% - Compiled VHDL code demonstration
     4% - Complete project demonstration on the FPGA platform
     5% - Project report

All the tutorials and projects could be done individually or in group of 2 students. Equipment should not be moved before, during or after the lab. In case if equipment seems to be defective it is a requirement to report to the lab instructor / technician who will take care of the problem.

Teaching Methods	The teaching method is based on: a) presentation the theory component in in-person lectures using the white board and slides; b) recommended self-learning materials: text book chapters and lab tutorials and c) implementation of the theory in the associated lab projects to provide practical hands-on experience in system-on-chip (SoC) design and functional verification using a) on-chip verification tools (e.g. Xilinx Chip-Scope) and platform tools (e.g. Logic Analysers, video-monitors, etc.).
Other Information	

Course Content

Week	Hours	Chapters / Section	Topic, description

1	3	B1: Ch.5/ 5.1	1. Introduction to COE 758: Scope and Objectives Management.
			2. Memory hierarchy and types of memory elements and their organization
			Read Book 1 Chapter 5 section 5.1 pp. 374-378
			    Book 2 Chapter 4 section 4.4 pp. 177-181
			    Book 3 Chapter 7 section 7.1 pp. 304-309

2	3	B1: Ch 5/ 5.2	Types of electronic memory and their organization:
			  1. Static and Dynamic Random Access Memory (RAM) structure and timing
			  2. Main memory components: DRAM EDO-DRAM SDRAM DDR-SDRAM RDRAM: structure, interface,timing
			 Read Book 1 Chapter 5 section 5.2 pp. 378-383
			    Book 3 Chapter 7 section 7.2 pp. 309-325

3	3	B1: Ch 5/ 5.3	Cache memory organization:
			  1. Principles of locality concepts terminology and organization of cache
			  2. Direct mapped cache: principles of operation and cache performance
			  3. Handling cache misses and writes. Cache & main memory coherence.
			 Read Book 1 Chapter 5 section 5.3 pp. 383-398
			    Book 2 Chapter 3 section 3.5.1 pp. 119-126
			    Book 3 Chapter 7 section 7.4 pp. 340-345

4	3	B1: Ch 5/ 5.4	Associative cache memory organization:
			  1. Ping-pong effect in direct mapped cache and cache efficiency
			  2. Two-way associative cache memory organization and operation
			  3. N-way associative cache: principles of operation pros and cons
			  4. Multi-level cache: concept organization and performance.
			 Read Book 1 Chapter 5 section 5.4 pp. 398-413

5	3	B1: Ch 5/ 5.7	Virtual memory: concept and organization:
			  1. Concept of memory virtualization terminology and general organization
			  2. Address translation page table and page replacement mechanism.
			 Read Book 1 Chapter 5 section 5.7 pp. 427-437
			    Book 2 Chapter 3 section 3.5.2 pp. 126-131
			    Book 3 Chapter 7 section 7.6 pp. 355-360

6	3	B1: Ch 5/ 5.7	Virtual memory: concept and organization:
			  1. Fast address translation in Translation Look aside Buffer (TLB)
			  2. Integrating virtual memory: TLB+cache+main memory+secondary storage.
			 Read Book 1 Chapter 5 section 5.7 pp. 438-453
			    Book 3 Chapter 7 section 7.6 pp. 361-365

7	2	B1: Ch 5 / 5.1 - 5.8	Midterm test: Preparation read: Book 1 Chapter 5 section 5.8 pp. 454-461

8	3	B3 Ch 8 / 8.1-8.3	Input-Output (I/O) subsystem organization:
			  1. Typical set of I/O devices in computing system
			  2. Interfacing processor(s) to I/O devices
			 Read Book 3 Chapter 8 sections 8.1-8.3 pp. 371-393

9	3	B3 Ch 9 / 9.1-9.3	Secondary data-storage devices: 1. Hard Disc Drive (HDD) principles of operation and performance

Week			
3			2. Solid State Drive (SSD) principles of operation and performance. Read Book 3 Chapter 9 sections 9.1-9.2 pp. 407-420

10	3	B3 Ch 9 / 9.4	Video-output subsystem organization:
			  1. Video-displays: principles of operation in graphical and character modes
			  2. Video-adaptors and video-processors: principles of operation and timing.
			Read Book 3 Chapter 9 section 9.4 pp. 421-429

11	3	B2 Ch 4 / 4.2	Buses: 1. Classification of buses synchronization and handshaking
			    2. Synchronous and asynchronous buses. Bus protocols and timing
			    3. Bus bandwidth calculation and methods for acceleration.
			Read Book 2 Chapter 4 section 4.3.1 pp. 165-171

12	3	B2 Ch 4 / 4.2	Bus arbitration and multi-level buses:
			  1. Bus arbitration mechanisms: Daisy-chain and centralized arbitration
			  2. Multi-level buses: Integration the memory bus and I/O buses
			  3. Direct memory Access (DMA): principles of operation and transfer modes.
			Read Book 2 Chapter 4 section 4.3.2 pp. 171-177
			    Book 3 Chapter 8 section 8.4 pp. 393-396

13	2	B3 Ch 8 /	Interaction between CPU I/O devices and memory:
			  1. Giving commands to I/O devices
			  2. Interrupt priority levels and interrupt service routines
			  3. Process of data transferring between CPU memory and I/O device.
			Book 3 Chapter 8 section 8.3 pp. 386-393

13	1		Review and Catch-up

Laboratory(L)/Tutorials(T)/Activity(A) Schedule

Week	L/T/A	Description
2	Tutorial	Introduction to Xilinx ISE CAD and FPGA development environment Reference tutorial: https://www.ee.ryerson.ca/~lkirisch/ele758/handouts/Tutorial1_ISE_Project_Creation.pdf
3	Project 1 Spec.	Tutorials: Design components in Xilinx Spartan FPGA. Project 1 Specification Reference tutorials: https://www.ee.ryerson.ca/~lkirisch/ele758/handouts/COE758_Digital_Design_Tutorial.pdf

		https://www.ee.ryerson.ca/~lkirisch/ele758/labs/Cache%20Project[12-09-10].pdf Read Book 1 Chapter 5 section 5.9 pp. 461-466
4	Project 1 Symbol	Creation of the symbol and block diagram of the Cache Controller SoC
5-6	Project 1 VHDL	VHDL-coding and compilation. Creation of simulation/hardware emulation environment and verification
7	Project 1 Demo	Complete project 1 demonstration and report submission
8	Project 2 Spec.	Introduction to video-processing systems and Project 2 specification
9	Project 2 Symbol	Creation of the symbol and block diagram of the Video-Game Processor SoC
10-11	Project 2 VHDL	VHDL-coding and compilation. Creation of simulation environment and verification
12	Project 2 Demo	Complete project 2 demonstration and report submission

University Policies

Students are reminded that they are required to adhere to all relevant university policies found in their online course shell in D2L and/or on the Senate website

Important Resources Available at Toronto Metropolitan University

- The Library provides research workshops and individual assistance. If the University is open, there is a Research Help desk on the second floor of the library, or students can use the Library's virtual research help service to speak with a librarian.
- Student Life and Learning Support offers group-based and individual help with writing, math, study skills, and transition support, as well as resources and checklists to support students as online learners.

- You can submit an Academic Consideration Request when an extenuating circumstance has occurred that has significantly impacted your ability to fulfill an academic requirement. You may always visit the Senate website and select the blue radio button on the top right hand side entitled: Academic Consideration Request (ACR) to submit this request.

   For Extenuating Circumstances, Policy 167: Academic Consideration allows for a once per semester ACR request without supporting documentation if the absence is less than 3 days in duration and is not for a final exam/final assessment. Absences more than 3 days in duration and those that involve a final exam/final assessment, require documentation. Students must notify their instructor once a request for academic consideration is submitted. See Senate Policy 167: Academic Consideration.

- If taking a remote course, familiarize yourself with the tools you will need to use for remote learning. The [Remote Learning Guide](#) for students includes guides to completing quizzes or exams in D2L Brightspace, with or without [Respondus LockDown Browser and Monitor, using D2L Brightspace,](#) joining online meetings or lectures, and collaborating with the Google Suite.
- Information on Copyright for [Faculty](#) and [students](#).

Accessibility

- Similar to an [accessibility statement,](#) use this section to describe your commitment to making this course accessible to students with disabilities. Improving the accessibility of your course helps minimize the need for accommodation.
- Outline any technologies used in this course and any known accessibility features or barriers (if applicable).
- Describe how a student should contact you if they discover an accessibility barrier with any course materials or technologies.

Academic Accommodation Support

Academic Accommodation Support (AAS) is the university's disability services office. AAS works directly with incoming and returning students looking for help with their academic accommodations. AAS works with any student who requires academic accommodation regardless of program or course load.

- Learn more about [Academic Accommodation Support](#).
- Learn [how to register with AAS](#).

Academic Accommodations (for students with disabilities) and Academic Consideration (for students faced with extenuating circumstances that can include short-term health issues) are governed by two different university policies. Learn more about [Academic Accommodations versus Academic Consideration and how to access each](#).

Wellbeing Support

At Toronto Metropolitan University, we recognize that things can come up throughout the term that may interfere with a student's ability to succeed in their coursework. These circumstances are outside of one's control and can have a serious impact on physical and mental well-being. Seeking help can be a challenge, especially in those times of crisis.

If you are experiencing a mental health crisis, please call 911 and go to the nearest hospital emergency room. You can also access these outside resources at anytime:

- **Distress Line:** 24/7 line for if you are in crisis, feeling suicidal or in need of emotional support (phone: 416-408-4357)
- **Good2Talk:** 24/7-hour line for postsecondary students (phone: 1-866-925-5454)
- **Keep.meSAFE:** 24/7 access to confidential support through counsellors via [My SSP app](#) or 1-844-451-9700

If non-crisis support is needed, you can access these campus resources:

- **Centre for Student Development and Counselling:** 416-979-5195 or email csdc@torontomu.ca
- **Consent Comes First - Office of Sexual Violence Support and Education:** 416-919-5000 ext 3596 or email osvse@torontomu.ca
- **Medical Centre:** call (416) 979-5070 to book an appointment

We encourage all Toronto Metropolitan University community members to access available resources to ensure support is reachable. You can find more resources available through the [Toronto Metropolitan University Mental Health and Wellbeing](#) website.