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## Faculty of Engineering and Architectural Science

Department of Electrical and Computer Engineering

**EE8217: Reconfigurable Computer Systems Engineering**

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**Prerequisites** None

**Course Web Page** [**http://www.ee.ryerson.ca/~lkirisch/ee8217/ee8217.htm**](http://www.ee.ryerson.ca/~lkirisch/ee8217/ee8217.htm)

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| **Compulsory Texts:** | | 1. Lev Kirischian, “Reconfigurable Computing Systems Engineering”, CRC Press, Taylor & Francis Group, ISBN-13: 978-1-4398-5621-5 2. Lecture notes from Dr. Lev G. Kirischian and recommended scientific papers. 3. Laboratory manual: Laboratory Manuals and Tutorials, Ryerson University. |
| **Calendar Description** | | This course is designed to offer an introduction in the theory and engineering design principles of the modern Reconfigurable Computing Systems (RCS) – one of the most rapidly growing sectors of the high-performance computer technology. The emphasis is in understanding of the concepts of architecture re-configurability, classes of RSC, sources for performance acceleration and cost-efficiency of RCS. Concept of resource virtualization in RCS is discussed in details as well as stages of synthesis of RCS architecture. The process of RCS development is described from the task algorithm / data structure analysis to virtual component synthesis, system integration and verification techniques. Additionally, the hardware basis of the modern RCS – fine and coarse-grained programmable logic devices: Field Programmable Gate Arrays (FPGA) and Coarse-Grained Reconfigurable Arrays (CGRA) will be overviewed.  The project portion of the course consists of: i) Literature research project and  ii) Design project based on Xilinx FPGA-based platform. This project assumes getting hands-on experience in RCS component synthesis and HDL-implementation, verification and comparative analysis with embedded software implementation. |
| **Learning Objectives** | | |  | | --- | | At the end of this course, the successful student will have a solid understanding of the concept of RCS and classification of RCS architectures, RCS organization, sources and methods for performance acceleration in RCS and cost-efficiency. The novel concept of virtualization of computing resources and entire architecture is another important aspect to be learned in this course. In the second part of the course students will learn the design methodology and get hands-on experience in development of RCS components, integration and verification techniques. | |  | |
| **Course Organization** | | 3hours of lecture per week for 13 weeks  2hours of lab per week for 7 weeks |
| **Course Evaluation** | Project 1: Literature survey - 25%  Project 2: RCS Component design - 25%  Final exam - 50%  \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_  Total 100%  To achieve a passing grade, student must pass both the theory and laboratory/project components. | |
| **Examinations** | Final examination is a 3-hour, closed-book examination that covers all the lecture materials. | |
| **Projects** | Project 1: Students are required to conduct literature research on one of areas associated with reconfigurable systems engineering. The project should include:   1. Investigation of the state-of-art in the selected area of interest,   b) Analysis on main directions of research in this area based on recent publications and  c) Formulation of main trends and / or classification of methods of RCS development and application.  The detailed structure of this project and list of suggested topics could be found at:  <http://www.ee.ryerson.ca/~lkirisch/ee8217/projects.htm>  Project 2: Students are required to perform the engineering design of an on-chip functional component from determination of functional and technical specification to complete design and verification. The on-chip hardware design should include:   1. Creation of component’s symbol and block-diagram of architecture; 2. Component’s HDL design, compilation, and physical implementation on the Xilinx Spartan FPGA based evaluation platform.; 3. Performance verification using on-chip logic analyzer (e.g. Xilinx Chip-Scope) should complete the design process.   In addition to the above, the comparison of performance between the designed hardware component and implementation in soft-core processor deployed in the same FPGA is required for analysis of component’s cost-performance efficiency.  The detailed structure of this project and list of suggested topics could be found at:  <http://www.ee.ryerson.ca/~lkirisch/ee8217/reports.htm> | |

**Course Content**

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| Week | Detailed Description | Hours | Reference |
| 1 | Computation process; Classification of computing systems and definition of Reconfigurable Computing Systems (RCS) | 3 | Chapter 1 |
| 2 | Classification of RCS architectures according to organization of the FCR:homogenous and heterogeneous architectures, fine-grain and coarse-grain systems, statically and dynamically reconfigurable RCS | 3 | Chapter 2 |
| 3-4 | FCR - Field of Configurable Resources: Architecture of the On-chip processing elements and communication infrastructure. | 6 | Chapter 3  & Chapter 4 |
| 5 | Application and specification analysis. High-level synthesis of RCS architecture: Segmentation of task algorithm and concept of Functional segment. Task segmentation methods. | 3 | Chapter 9: 9.1 to 9.5 |
| 6 | Implementation of Functional Segments: Concept of Virtual Components. Determination of component’s nature (HW or SW). Determination of component interface and synchronization scheme | 3 | Chapter 9: 9.6 |
| 7 | Cost-efficiency of RCS: Performance-Cost Ratio (PCR) and cost-efficiency, Performance-Cost Ratio (PCR) calculation. Methods for Increasing cost-efficiency by partitioning the workload . | 3 | Lecture notes |
| 8 | Methods for performance acceleration in RCS: Sources of parallelism in task algorithm and data structure. Sources for virtual hardware component (VHC) performance acceleration. | 3 | Chapter 9: 9.7 & 9.8 |
| 9-10 | High-level synthesis of hardware component: Main stages of process: creation of sequencing graph (SG), scheduling, binding and getting data-path block diagram of the VHC. | 6 | Chapter 9:  9.9 – 9.12 |
| 11-12 | RCS architecture integration: Concept of Application Specific Virtual Processors (ASVP). Integration of ASVP in time domain (temporal partitioning) and in spatial domain (spatial partitioning) | 6 | Chapter 10 |
| 13 | Course review and final examination | 3 | 3 |

**Important Notes**

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| 1. All of the required course-specific written reports will be assessed not only on their technical/academic merit, but also on the communication skills exhibited through these reports. 2. All assignment and lab/tutorial reports must have the standard cover page which can be completed and printed from the Department website at www.ee.ryerson.ca. The cover page must be signed by the student(s) prior to submission of the work. Submissions without the cover pages **will not** be accepted. |

3. Should a student miss a mid-term test or equivalent (e.g. studio or presentation), with appropriate documentation, a make-up will be scheduled as soon as possible in the same semester. Make-ups should cover the same material as the original assessment but need not be of an identical format. Only if it is not possible to schedule such a make-up may the weight of the missed work be placed on the final exam, or another single assessment. This may not cause that exam or assessment to be worth more than 70% of the student’s final grade. If a student misses a scheduled make-up test or exam, the grade may be distributed over other course assessments even if that makes the grade on the final exam worth more than 70% of the final grade in the course.

4. Students who miss a final exam for a verifiable reason and who cannot be given a make-up exam prior to the submission of final course grades, must be given a grade of INC (as outlined in the *Grading Promotion and Academic Standing Policy)* and a make-up exam (normally within 2 weeks of the beginning of the next semester) that carries the same weight and measures the same knowledge, must be scheduled.

5. Medical or Compassionate documents for the missing of an exam must be submitted within 3 working days of the exam. Students are responsible for notifying the instructor that they will be missing an exam as soon as possible.

6. Requests for accommodation of specific religious or spiritual observance must be presented to the instructor no later than two weeks prior to the conflict in question (in the case of final examinations within two weeks of the release of the examination schedule). In extenuating circumstances this deadline may be extended. If the dates are not known well in advance because they are linked to other conditions, requests should be submitted as soon as possible in advance of the required observance. Given that timely requests will prevent difficulties with arranging constructive accommodations, students are strongly encouraged to notify the instructor of an observance accommodation issue within the first two weeks of classes.

7. The results of the first test or mid-term exam will be returned to students before the deadline to drop an undergraduate course in good Academic Standing.

8. Students are required to adhere to all relevant University policies including:

Undergraduate Grading, Promotion and Academic Standing, <http://www.ryerson.ca/senate/policies/pol46.pdf>

Student Code of Academic Conduct, <http://www.ryerson.ca/senate/policies/pol60.pdf>

Student Code of Non-Academic Conduct, <http://www.ryerson.ca/senate/policies/pol61.pdf>

Undergraduate Academic Consideration and Appeals, <http://www.ryerson.ca/senate/policies/pol134.pdf>

Examination Policy, <http://www.ryerson.ca/senate/policies/pol135.pdf>

Accom. of Student Relig., Abor. And Spir. Observance, <http://www.ryerson.ca/senate/policies/pol150.pdf>

Est. of Stud. Email Accts for Official Univ. Commun., <http://www.ryerson.ca/senate/policies/pol157.pdf>

9. Students are required to obtain and maintain a Ryerson Matrix e-mail account for timely communications between the instructor and the students.

10. Any changes in the course outline, test dates, marking or evaluation will be discussed in class prior to being implemented.

11. In-class use of cellular telephones is not permitted. Please turn off your cell phone prior to class. Quiet use of laptops, text-messengers and similar non-audible devices are permitted only in the rear rows of the class. This restriction allows use of such devices by their users while limiting audible and visual distractions to other students. This policy may change without notice.

12. Labs, projects handed in past the due date and time will not be accepted for marking and will receive a mark of ZERO. In some genuine cases late submission will be allowed with a penalty of 5% per day.

13. Students found to have plagiarized *any* portion of their labs and final project will receive a grade of zero on the *complete* project. This automatically will lead to a failing grade

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| Name of Instructor | Lev Kirischian | Signature of Instructor |  | Date |  |
| Name of Graduate Program Director |  | Signature of Graduate Program Director |  | Date |  |