Faculty Name: Andy Gean Ye

Project Title: Silicon Level Layout and Design of Digital Circuits

Description of Project (Provide ½ page project description)

A 2, 3, or 4th year Electrical/Computer engineering student is needed for a research assistantship position in the area of design and layout of digital circuits at silicon level. The student will be responsible for the silicon level layout of transistor structures using Cadenece tools and Hspice. Training will be provided.

Responsibility of Student (Specify the duties and responsibilities of the student)

Please see Project Description.

Specify Requirements (Please state any specific requirement of this position)

Desired Skills:
Good knowledge of Spice.
Good knowledge of Digital Circuits.
Good knowledge in FPGA programming techniques using VHDL/Verilog in Altera/Xilinx.

Desired Academic Background Preparation:

Good background preparation in ELE404 (Electronics I), ELE202 (Electric Circuit), ELE302 (Electric Networks) and COE328 (Digital Systems). Good performance in ELE734 will be a plus for 4th year students.
2015 Research Internship