Faculty of Engineering, Architecture and Science
Department of Electrical and Computer Engineering

Course Outline

COE838: Systems-on-Chip Design

Prerequisites

COE718 or ELE734

Course Web Page

http://www.ee.ryerson.ca/~courses/coe838/

All course related information, announcements and material such as lab documents are available at the course website.

Compulsory Texts:


Laboratory/Project Manuals and Documents: Available through the course web page: http://www.ee.ryerson.ca/~courses/coe838

Reference Texts:


Some relevant review articles to be identified by the instructor and will be available at the course web page and/or from the library.

Calendar Description

This course will cover the advance topics of system-on-chip (SoC) design, hardware-software co-specification, co-synthesis, network-on-chip (NoC) systems and system-on-programmable-chip technologies. It provides the advance knowledge required for system-on-chip design and development, multi-core architectures and embedded systems on a chip. Students will also be introduced to the main principles of system-on-chip modeling and design using SystemC. SystemC will be employed to present a unified (Hardware and Software) view of various SoC components. Some SoC soft processor cores such as Nios-II, ARM Cortex-A9, etc and other SoC IPs will be studied and various design tools including Quartus II and other tools will be utilized in the projects. Interconnection structures suitable for SoC design will be studied. On-chip busses (e.g. AMBA, Avalon, IBM Core-connect, etc.) and network-on-chip techniques will be covered in detail. After introducing hardware-software co-design related tools and NoC architectures, various applications’ case studies will be explored.

Learning Objectives

At the end of this course, the successful student will be able to:

1. Interconnect engineering concepts related to soft-processor cores, hardware and software systems to design an SoC for real-world applications. Learn to employ specialized knowledge of subsystems like processor cores and other SoC components to design an embedded SoC. (1c) and (1d)

Assessment Methods: Midterm or Final examinations and some Labs and the course project.

2. Improve students’ capabilities of using the technical knowledge of processor architecture, peripherals, programming, and CAD tools to design application specific
SoCs. Solve various challenges of high performance SoC design in multiple stages by employing hardware/software co-design methodologies to test and verify each stage and then integrate different stages into an efficient SoC architecture. (4a) and (4c).

**Assessment Methods:** Labs and course project as well as final examination.

3. Learn and efficient use of different SoC simulation, modeling and prototyping tools including SystemC, QSys and Quartus-II. These tools facilitate co-simulation and co-design of SoCs. (5c)

**Assessment Methods:** Labs and the course project.

4. Demonstrate the main features of the course-project and answer critical and project specific questions during project demo and oral sessions. Write project report by following a standard IEEE paper like format, where all the lab and project reports are evaluated based on their completeness, English, and citations. (7a) and (7b)

**Assessment Methods:** Labs and the course project.

Note: Numbers in parentheses refer to the graduate attributes required by the Canadian Engineering Accreditation Board. For more information, see: [http://www.feas.ryerson.ca/quality_assurance/accreditation.pdf](http://www.feas.ryerson.ca/quality_assurance/accreditation.pdf)

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**Course Organization**

<table>
<thead>
<tr>
<th>Course Organization</th>
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<tbody>
<tr>
<td>3 hours of lecture per week for 13 weeks, in 2 sections</td>
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<tr>
<td>1 hours of lab per week for 12 weeks</td>
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<tr>
<td>2 Lab sections of a maximum of 20 students</td>
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<td>1 Teaching Assistant (TA), 2 sections per TA</td>
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**Course Evaluation**

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<tr>
<th>Course Evaluation</th>
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<tbody>
<tr>
<td>Midterm exam</td>
<td>25%</td>
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<tr>
<td>Labs and Project</td>
<td>35%</td>
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<tr>
<td>Final exam</td>
<td>40%</td>
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<tr>
<td>Total</td>
<td>100%</td>
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- To achieve a passing grade, student must pass both the theory and laboratory/project components. Labs are mainly organized for SoC design using SystemC and SoC tools and system partitioning techniques.
- Individual and team projects cover SoC design and modeling.

**Examinations**

Midterm exam in Week 8 or 9, 1.5 hours, closed book (covers Weeks 1-8 of lecture and laboratory material).

Final exam, during exam period, 2 hours, closed book (covers all the course material).

**Project**

Each project combines three separate components: a written component, a demonstration/presentation component and an oral component. It is an individual project but depending on the extended project selection, and with the consent of the instructor multiple students are allowed to undertake complex projects.

Project marks will be awarded out of 100 marks as per following schedule:

- Summary of Project (1-2 pages). Week 5. 5% Marks
- Demo of project progress in Week-8 lab session. 10% Marks
- Interim project report (4-6 typed pages). Start of week-10. 20% Marks
- Final demonstration, oral and presentation. Weeks-11 and 12 lab sessions. 30% Marks
- Final project report. Week 13. 35% Marks

**Project Report Format**

Final report of the project should be of 10-15 pages with the following IEEE like format.

1. The report must be typed and have some Figures and/or drawings of your own.
2. Avoid Cut and paste of Figures from other papers or manuals.
3. A suitable Font (Bookman, Courier, Times New Roman) of size 11 or 12 points.
4. Single line spacing.
5. Pages of letter size with 1.0" top, bottom, left and right margins.
6. The report must have the following sections:
   Introduction, Past Work or Review, Methodology, SoC Modeling, SoC Design, Conclusions, Reference. You can always have some more sections such as Appendix, etc.

**Course Content**

<table>
<thead>
<tr>
<th>Week</th>
<th>Detailed Description</th>
<th>Hours</th>
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<tbody>
<tr>
<td>1</td>
<td>Introduction to System on Chip (SoC) -- An SoC Design Approach</td>
<td>3</td>
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<tr>
<td>2</td>
<td>Introduction to SystemC. Using SystemC for SoC Co-specification</td>
<td>3</td>
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<tr>
<td>3</td>
<td>SystemC based Performance Modeling and Analysis of SoCs</td>
<td>3</td>
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<tr>
<td>4</td>
<td>Basics of Chips and SoC ICs: Cycle Time, Die Area-and-Cost, Power, Area-time-Power Tradeoffs and Chip Reliability</td>
<td>3</td>
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<tr>
<td>5</td>
<td>SoPC (System on Programmable Chips) and SoC Design</td>
<td>3</td>
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<tr>
<td>6</td>
<td>Hardware Software Co-synthesis of SoC Applications</td>
<td>3</td>
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<tr>
<td>7</td>
<td>SoC processors and their Selections Various Processor Soft Cores: Nios-II, ARM Cortex-A9, OpenRISC, Leon4, OpenSPARC</td>
<td>3</td>
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<tr>
<td>8</td>
<td>SoC Interconnection Structures <strong>Mid-term Exam</strong></td>
<td>3</td>
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<tr>
<td>9</td>
<td>On-Chip Busses: AMBA, Core-connect, Avalon, etc.</td>
<td>3</td>
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<tr>
<td>10</td>
<td>NoC (Network on Chip) based Interconnection. Regular (Mesh, Torus, Tree, etc.) and Application Specific NoC Topologies. Comparing on-chip Bus interconnection with NoCs.</td>
<td>3</td>
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<tr>
<td>11</td>
<td>Multi-core and MPSoc (Multiprocessor SoC) Architectures</td>
<td>3</td>
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<tr>
<td>12</td>
<td>Introduction to SoC Memory Design SoC Application Case Studies</td>
<td>3</td>
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<tr>
<td>13</td>
<td>Catching up and Review</td>
<td>3</td>
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**Laboratory/Projects - Room ENG: 408/412**

<table>
<thead>
<tr>
<th>Labs. Project</th>
<th>Detailed Description</th>
<th>Week</th>
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<tbody>
<tr>
<td>1</td>
<td>SystemC: Introduction and Tutorial</td>
<td>2</td>
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<tr>
<td>2</td>
<td>SoC Modeling using SystemC</td>
<td>3</td>
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<tr>
<td>3</td>
<td>Multiprocessor System on Chip Design and Implementation</td>
<td>4-5</td>
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<tr>
<td>Project</td>
<td>Students are required to investigate, model, design and prototype an SoC for a typical application such as multimedia, biomedical, communication, smart-home, automotive and other industrial applications. An on-line project presentation and a formal professionally written project report are due at the end of the term.</td>
<td>6-12</td>
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**Note:** There is a 5% per day penalty of marks for late submission of labs or project. Individual and team projects are organized related to modeling and design of SoCs.

**Note:** Schedule of lectures and labs is tentative. There may be some changes in the schedule that will be announced in the class and posted at the course website.
Important Notes
1. All of the required course-specific written reports will be assessed not only on their technical/academic merit, but also on the communication skills exhibited through these reports.
2. All assignment and lab/tutorial reports must have the standard cover page which can be completed and printed from the Department website at www.ee.ryerson.ca. The cover page must be signed by the student(s) prior to submission of the work. Submissions without the cover pages will not be accepted.
3. Should a student miss a mid-term test or equivalent (e.g. studio or presentation), with appropriate documentation, a make-up will be scheduled as soon as possible in the same semester. Make-ups should cover the same material as the original assessment but need not be of an identical format. Only if it is not possible to schedule such a make-up may the weight of the missed work be placed on the final exam, or another single assessment. This may not cause that exam or assessment to be worth more than 70% of the student’s final grade. If a student misses a scheduled make-up test or exam, the grade may be distributed over other course assessments even if that makes the grade on the final exam worth more than 70% of the final grade in the course.
4. Students who miss a final exam for a verifiable reason and who cannot be given a make-up exam prior to the submission of final course grades, must be given a grade of INC (as outlined in the Grading Promotion and Academic Standing Policy) and a make-up exam (normally within 2 weeks of the beginning of the next semester) that carries the same weight and measures the same knowledge, must be scheduled.
5. Medical or Compassionate documents for the missing of an exam must be submitted within 3 working days of the exam. Students are responsible for notifying the instructor that they will be missing an exam as soon as possible.
6. Requests for accommodation of specific religious or spiritual observance must be presented to the instructor no later than two weeks prior to the conflict in question (in the case of final examinations within two weeks of the release of the examination schedule). In extenuating circumstances this deadline may be extended. If the dates are not known well in advance because they are linked to other conditions, requests should be submitted as soon as possible in advance of the required observance. Given that timely requests will prevent difficulties with arranging constructive accommodations, students are strongly encouraged to notify the instructor of an observance accommodation issue within the first two weeks of classes.
7. The results of the first test or mid-term exam will be returned to students before the deadline to drop an undergraduate course in good Academic Standing.
8. Students are required to adhere to all relevant University policies including:
9. Students are required to obtain and maintain a Ryerson Matrix e-mail account for timely communications between the instructor and the students.
10. Any changes in the course outline, test dates, marking or evaluation will be discussed in class prior to being implemented.
11. In-class use of cellular telephones is not permitted. Please turn off your cell phone prior to class. Quiet use of laptops, text-messengers and similar non-audible devices are permitted only in the rear rows of the class. This restriction allows use of such devices by their users while limiting audible and visual distractions to other students. This policy may change without notice.
12. Labs, projects handed in past the due date and time will not be accepted for marking and will receive a mark of ZERO. In some genuine cases late submission will be allowed with a penalty of 5% per day.
13. Students found to have plagiarized any portion of their labs and final project will receive a grade of zero on the complete project. This automatically will lead to a failing grade.

Course Coordinator __________________________                Date ________________________________

Approved by _______________________________                Date ________________________________

Program Director
or Department Chair