Course Outline

ELE202: Electric Circuits Analysis

Prerequisites  MTH 140 and MTH 141

Program Level  ELE02 (2nd Semester)

Course Web Page  http://www.ee.ryerson.ca/~courses/ele202/, found on Blackboard

Compulsory Texts:


Laboratory Manual:


Calendar Description

This course is a one semester introductory course in electric circuit analysis. The topics covered include the following: circuit variables and elements, resistive circuits, methods of circuit analysis, circuit theorems, energy storage elements, transient responses of RL and RC circuits, sinusoidal steady state analysis, and AC steady state power concepts.

Learning Objectives

At the end of this course, the successful student will be able to:

**Attribute 1. Knowledge Base for Engineering**

1. Understands, interprets, articulates, and applies the basic voltage and current laws in the identification, formulation, and solution of the basic problem of circuit analysis. (1a: Natural Sciences)

   **Assessment Methods**: Directly assessed in quiz, midterm, and final examination.

   **Assessment Measures**: During the quiz, midterm, and final examination, the students will be asked to solve a series of circuits using one of the standard circuit analysis methods.

2. Develops linear equations based on different circuit configurations. Solve linear equations using variable elimination or Cramer rule. (1b: Mathematics)

   **Assessment Methods**: Directly assessed in quiz, midterm, and final examination.

   **Assessment Measures**: During the quiz, midterm, and final examination, the students will be asked to solve a series of circuits using one of the standard circuit analysis methods, which extrapolate a set of linear equations based on circuit topologies. Questions might explicitly ask students to solve these equations using either variable elimination or Cramer rule.

**Attribute 2. Problem Analysis**

3. Conducts experiments using the basic principles of circuit analysis and analyze and interpret the obtained results. (2a: Processing)

   **Assessment Methods**: Directly assessed based on laboratory performances.

   **Assessment Measures**: Students are given a checklist of circuit variables to measure and rubric ahead of time. Students must accurately measure the required
circuit variables and is marked based on the correctness of the measurements.

**Attribute 5. Use of Engineering Tools**

4. Uses current and voltage measurement instruments, including volt/current meters and oscilloscope to measure the voltage and current characteristics of various circuits. (5a: Conducting experiments/measurement)

**Assessment Methods:** Directly assessed based on laboratory assignments.

**Assessment Measures:** Students are given a checklist of circuit variables to measure and rubric ahead of time. Students must accurately measure the required circuit variables and is marked based on the correctness of the measurements.

5. Follows the safety protocols and procedures when dealing with voltage and current sources. (5a: Conducting experiments/measurement)

**Assessment Methods:** Directly assessed based on the lab safety test given at the start of the term.

**Assessment Measures:** During the lab safety test, students must correctly answer all lab safety related questions before they can start their first experiment.

Note: Numbers in parentheses refer to the graduate attributes required by the Canadian Engineering Accreditation Board. For more information, see:

Course Organization

4 hours of lecture per week for 13 weeks.
1.5 hours of lab per week for 13 weeks.
0.5 hours of tutorial per week for 13 weeks.

Course Evaluation

<table>
<thead>
<tr>
<th>Component</th>
<th>Weight</th>
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<tbody>
<tr>
<td>Quiz</td>
<td>5%</td>
</tr>
<tr>
<td>Midterm Test</td>
<td>25%</td>
</tr>
<tr>
<td>Final Exam</td>
<td>50%</td>
</tr>
<tr>
<td>Lab Reports</td>
<td>10%</td>
</tr>
<tr>
<td>Lab Projects</td>
<td>10%</td>
</tr>
<tr>
<td>Total</td>
<td>100%</td>
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</tbody>
</table>

- To achieve a passing grade, student must pass both the theory and laboratory/project components.
- All quizzes, mid-term test and final examination will be closed book. Only the non-programmable approved calculator (Sharp EL546 or Casio fx-991MS and their later models) will be allowed.
- All lab reports will be assessed not only on their technical merits, but also on the communication skills of the students.

Examinations

Midterm exam in Week 8, 1.5 hours, closed book (covers Weeks 1-6 of lecture and laboratory material).
Final exam, during exam period, 3 hours, closed book (covers all the course material).

Course Content

<table>
<thead>
<tr>
<th>Week</th>
<th>Lecture Topic (Lecture Hours)</th>
<th>Experiment/Tutorial</th>
</tr>
</thead>
<tbody>
<tr>
<td>Week-1</td>
<td>Basic Concepts (4)</td>
<td>No Lab or Tutorial</td>
</tr>
<tr>
<td>Jan 5 – Jan 11, 2015</td>
<td>Chap-1, sections: 1.1 to 1.7</td>
<td></td>
</tr>
<tr>
<td>Week-2</td>
<td>Basic Laws (4)</td>
<td>Expt-1</td>
</tr>
<tr>
<td>Jan 12 – Jan 18, 2015</td>
<td>Chap-2, sections: 2.1 to 2.8</td>
<td>Simple DC circuit</td>
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<tr>
<td>Week-3</td>
<td>Methods of Analysis (4)</td>
<td>Tutorial/Quiz</td>
</tr>
<tr>
<td>Jan 19 – Jan 25, 2015</td>
<td>Chap-3, sections: 3.1 to 3.3</td>
<td>Chap-1, 2</td>
</tr>
<tr>
<td>Week-4</td>
<td>Methods of Analysis (4)</td>
<td>Expt-2</td>
</tr>
<tr>
<td>Jan 26 – Feb 1, 2015</td>
<td>Chap-3 (continued), sections: 3.4 to 3.7</td>
<td>General DC circuit</td>
</tr>
<tr>
<td>Week-5</td>
<td>Circuit Theorems (4)</td>
<td>Tutorial/Quiz</td>
</tr>
<tr>
<td>Feb 2 – Feb 8, 2015</td>
<td>Chap-4, sections: 4.1 to 4.5</td>
<td>Chap-3</td>
</tr>
<tr>
<td>Week-6</td>
<td>Circuit Theorems (4)</td>
<td>Expt-4</td>
</tr>
<tr>
<td>Feb 9 – Feb 15, 2015</td>
<td>Chap-4 (continued), section: 4.6 to 4.8, and 4.10</td>
<td>Introduction to Scopes</td>
</tr>
<tr>
<td>Reading Week</td>
<td>Reading Week</td>
<td>Reading Week</td>
</tr>
<tr>
<td>Feb 16 – Feb 22, 2015</td>
<td></td>
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<tr>
<td>Week-7</td>
<td>Capacitors and Inductors (4)</td>
<td>Tutorial/Quiz</td>
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<tr>
<td>Feb 23 – Mar 1, 2015</td>
<td>Chap-6, sections: 6.1 to 6.5</td>
<td>Chap-4</td>
</tr>
</tbody>
</table>

Mid-Term Test Wed Feb 25, 2015
| Week-8  
Mar 2 – Mar 8, 2015 | First-Order Circuits (4)  
Chap-7, section: 7.1 to 7.4 | Expt-3  
Thevenin’s circuit & Max. power transfer |
|---------------------|--------------------------|------------------------------------------|
| Week-9  
Mar 9 – Mar 15, 2015 | First-Order Circuits (4)  
Chap-7 (continued), sections: 7.5, 7.6 and 7.9 | Expt-5  
Pulse response of RC & RL circuits |
|---------------------|--------------------------|------------------------------------------|
| Week-10  
Mar 16 – Mar 22, 2015 | Sinusoids and Phasors (4)  
Chap-9, sections: 9.1 to 9.4 | Tutorial/Quiz  
Chap 6 & 7 |
|---------------------|--------------------------|------------------------------------------|
| Week-11  
Mar 23 – Mar 29, 2015 | Sinusoids and Phasors (4)  
Chap-9 (continued), sections: 9.5 to 9.8 | Expt-6  
Sinusoidal-Steady-State Response of RC & RL Circuits |
|---------------------|--------------------------|------------------------------------------|
| Week-12  
Mar 30 – Apr 5, 2015 | Sinusoidal Steady-State Analysis (4)  
Chap-10, sections: 10.1 to 10.6 | Tutorial/Quiz  
Chap 9 |
|---------------------|--------------------------|------------------------------------------|
| Week-13  
Apr 6 – Apr 12, 2015 | AC Power Analysis (4)  
Chap-11: section 11.1 to 11.2, 11.4 to 11.6 and REVIEW  
Last class: Thu April 10, 2014 | Lab Project(mystery box) |

Laboratory/Projects - Room ENG301/ENG302

<table>
<thead>
<tr>
<th>Labs.</th>
<th>Detailed Description</th>
<th>Week</th>
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| 1     | **Simple DC Circuit:**  
[Familiarity with DMM, Voltmeter & Ammeter; Measure linear/non-linear i-v characteristic of different devices; verification of Kirchhoff’s laws] | 2 |
| 2     | **General DC Circuit:**  
[Familiarity with (reference point) ground; investigate performance of a general DC circuit; Design, construct and test a simple voltage divider] | 4 |
| 3     | **Thevenin’s Circuit & Max. Power Transfer:**  
[Develop, construct and test performance of a Thevenin’s equivalent two-terminal source-network with variable load; Evaluate effects of load variation at source-load interface] | 6 |
| 4     | **Introduction to Scopes:**  
[More advanced usage of DMM; Familiarity with Oscilloscopes and Function Generators] | 8 |
| 5     | **Pulse Response of RC & RL Circuits:**  
[Measure internal resistance of function generator; investigate dynamic response of simple RC/RL circuits due to pulse excitation] | 9 |
| 6     | **Sinusoidal-Steady-State Response of RC & RL Circuits:**  
[Examine SSS response of simple RC & RL circuits; investigate effect of frequency variations on amplitude and phase angle of SSS response] | 11 |

**Note:** Schedule of lectures and labs is tentative. There may be some changes in the schedule that will be announced in the class and posted at the course website.

**Important Notes**
1. All of the required course-specific written reports will be assessed not only on their technical/academic merit, but also on the communication skills exhibited through these reports.

2. All assignment and lab/tutorial reports must have the standard cover page which can be completed and printed from the Department website at www.ee.ryerson.ca. The cover page must be signed by the student(s) prior to submission of the work. Submissions without the cover pages will not be accepted.

3. Should a student miss a mid-term test or equivalent (e.g. studio or presentation), with appropriate documentation, a make-up will be scheduled as soon as possible in the same semester. Make-ups should cover the same material as the original assessment but need not be of an identical format. Only if it is not possible to schedule such a make-up may the weight of the missed work be placed on the final exam, or another single assessment. This may not cause that exam or assessment to be worth more than 70% of the student’s final grade. If a student misses a scheduled make-up test or exam, the grade may be distributed over other course assessments even if that makes the grade on the final exam worth more than 70% of the final grade in the course.

4. Students who miss a final exam for a verifiable reason and who cannot be given a make-up exam prior to the submission of final course grades, must be given a grade of INC (as outlined in the Grading Promotion and Academic Standing Policy) and a make-up exam (normally within 2 weeks of the beginning of the next semester) that carries the same weight and measures the same knowledge, must be scheduled.

5. Medical or Compassionate documents for the missing of an exam must be submitted within 3 working days of the exam. Students are responsible for notifying the instructor that they will be missing an exam as soon as possible.

6. Requests for accommodation of specific religious or spiritual observance must be presented to the instructor no later than two weeks prior to the conflict in question (in the case of final examinations within two weeks of the release of the examination schedule). In extenuating circumstances this deadline may be extended. If the dates are not known well in advance because they are linked to other conditions, requests should be submitted as soon as possible in advance of the required observance. Given that timely requests will prevent difficulties with arranging constructive accommodations, students are strongly encouraged to notify the instructor of an observance accommodation issue within the first two weeks of classes.

7. The results of the first test or mid-term exam will be returned to students before the deadline to drop an undergraduate course in good Academic Standing.

8. Students are required to adhere to all relevant University policies including:

9. Students are required to obtain and maintain a Ryerson Matrix e-mail account for timely communications between the instructor and the students.

10. Any changes in the course outline, test dates, marking or evaluation will be discussed in class prior to being implemented.

11. In-class use of cellular telephones is not permitted. Please turn off your cell phone prior to class. Quiet use of laptops, text-messengers and similar non-audible devices are permitted only in the rear rows of the class. This restriction allows use of such devices by their users while limiting audible and visual distractions to other students. This policy may change without notice.

12. Labs, projects handed in past the due date and time will not be accepted for marking and will receive a mark of ZERO. In some genuine cases late submission will be allowed with a penalty of 5% per day.

13. Students found to have plagiarized any portion of their labs and final project will receive a grade of zero on the complete project. This automatically will lead to a failing grade.