## Instructor(s)

<table>
<thead>
<tr>
<th>Instructor</th>
<th>Office</th>
<th>Phone</th>
<th>Email</th>
<th>Office Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reza Sedaghat</td>
<td>ENG431</td>
<td>(416) 979-5000 x 6083</td>
<td><a href="mailto:rsedagha@ryerson.ca">rsedagha@ryerson.ca</a></td>
<td>TBA</td>
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<tr>
<td>Vadim Geurkov</td>
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</tr>
<tr>
<td>Nagi Mekhiel</td>
<td>ENG446</td>
<td>(416) 979-5000 x 7251</td>
<td><a href="mailto:nmekhiel@ryerson.ca">nmekhiel@ryerson.ca</a></td>
<td>TU 11-12, Th 10-11</td>
</tr>
<tr>
<td>Prathap Siddavaatam</td>
<td>TBA</td>
<td>TBA</td>
<td><a href="mailto:prathap.siddavaatam@ryerson.ca">prathap.siddavaatam@ryerson.ca</a></td>
<td>TBA</td>
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## Calendar Description

This course covers the basics digital logic circuits and emphasizes on good understanding of basic concepts in modern digital system design. The course introduces computer aided design (CAD) tools including the use of hardware description language (HDL) for design entry. It also discusses the use of the latest available implementation technologies including CPLDs and FPGAs for mapping the design to modern technology. This course covers basic logic circuits, Boolean algebra, and implementation technology (from transistor to CPLDs and FPGAs). It also introduces logic functions optimization and implementation, number representation and arithmetic circuits, combinational circuits, synchronous and asynchronous sequential circuits as well as introduction to control unit data path and CPU operations. The Laboratory work requires the uses of CAD tools to design and simulate basic digital circuits. Implementation and testing of simple digital systems in LSI and CPLD will also be considered. (Formerly ELE 328.)

## Prerequisites

- CPS 125, and ELE 202 and MTH 240

## Antirequisites

- BME 328

## Corequisites

- None

## Compulsory Text(s):

3. Laboratory Manual: Available through the course web page: http://www.ee.ryerson.ca/~courses/ees508

## Reference Text(s):

At the end of this course, the successful student will be able to:

1. The theoretical and technical knowledge of design methodology from the lecture will be applied in the labs using design tools (Altera® Quartus® II, Altera® FPGA boards) for analysis, simulation, visualization, synthesis, and design. Modern instrumentation such as logic analyzer, oscilloscope, etc. will be utilized to collect and validate the digital data. Learning various mathematical models and design methods for digital systems, such as Boolean algebra and optimization design strategies, gives the student the ability to solve principle engineering problems Selects and uses an appropriate method for problem definition. Describes differences between methods, performs a specified method in hypothetical design situation. (4a)

2. Learning various mathematical models and design methods for digital systems, such as Boolean algebra and optimization design strategies, gives the student the ability to solve principle engineering problems Selects and uses an appropriate method for problem definition. Describes differences between methods, performs a specified method in hypothetical design situation. (4b)

3. The student has to submit a report in Lab 7. S/He must read and appropriately responds to technical and non-technical instructions. (7a)

NOTE: Numbers in parentheses refer to the graduate attributes required by the Canadian Engineering Accreditation Board (CEAB).

### Course Organization

<table>
<thead>
<tr>
<th>Course Organization</th>
<th>4.0 hours of lecture per week for 13 weeks</th>
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<tbody>
<tr>
<td></td>
<td>3.0 hours of lab/tutorial per week for 12 weeks</td>
</tr>
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</table>

### Teaching Assistants

| Teaching Assistants | TBA |

### Course Evaluation

<table>
<thead>
<tr>
<th>Theory</th>
<th>Midterm Exam 25 %</th>
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<tbody>
<tr>
<td></td>
<td>Final Exam 45 %</td>
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<tr>
<td>Laboratory</td>
<td></td>
</tr>
<tr>
<td>Lab Work</td>
<td>30 %</td>
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<tr>
<td>TOTAL:</td>
<td>100 %</td>
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### Examinations

- Midterm exam in Week 7, two hours, problems, closed book (covers Weeks 1-6).
- Final exam, during exam period, two hours, closed-book (covers Weeks 8-13).

### Other Evaluation Information

- None

### Other Information

- None

### Course Content

<table>
<thead>
<tr>
<th>Week</th>
<th>Hours</th>
<th>Chapters / Section</th>
<th>Topic, description</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>4</td>
<td>INTRODUCTION TO COE328</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>4</td>
<td>INTRODUCTION TO LOGIC CIRCUITS (Chapter 2 Sections 2.1 to 2.10)</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>4</td>
<td>IMPLEMENTATION TECHNOLOGY (Chapter 3 Sections 3.1 to 3.10)</td>
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</table>
OPTIMIZATION OF COMBINATIONAL LOGIC
(Chapter 4 Sections 4.2 to 4.12)

NUMBER REPRESENTATION AND ARITHMETIC CIRCUITS
(Chapter 5 Sections 5.1 to 5.8)

COMBINATIONAL CIRCUIT BUILDING BLOCKS
(Chapter 6 Sections 6.1 to 6.6)

INTRODUCTION TO SEQUENTIAL CIRCUITS
(Chapter 7 Sections 7.1 to 7.13)

SYNCHRONOUS SEQUENTIAL CIRCUITS
(Chapter 8 Sections 8.1 to 8.9)

ASYNCHRONOUS SEQUENTIAL CIRCUITS
(Chapter 9 Sections 9.1 to 9.6)

REGISTER-LEVEL DESIGN
(Chapter 8 Sections 8.1 to 8.6)

SYSTEM ARCHITECTURE
(Chapter 9 Sections 9.1 to 9.4)

Laboratory/Tutorials/Activity Schedule

<table>
<thead>
<tr>
<th>Week</th>
<th>Lab</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-3</td>
<td>ENG306-7</td>
<td>CAD Tools Tutorial</td>
</tr>
<tr>
<td>4</td>
<td>ENG306-7</td>
<td>Functional Implementation and Minimization</td>
</tr>
<tr>
<td>5-6</td>
<td>ENG306-7</td>
<td>Adder and Subtractor Unit</td>
</tr>
<tr>
<td>7-8</td>
<td>ENG306-7</td>
<td>Combinational Circuits and Storage Elements</td>
</tr>
<tr>
<td>9-10</td>
<td>ENG306-7</td>
<td>Sequential Circuits: Implementing an Eight State Machine</td>
</tr>
<tr>
<td>11-13</td>
<td>ENG306-7</td>
<td>Design of a Simple Processor Module</td>
</tr>
</tbody>
</table>

Policies & Important Information:

1. Students are required to obtain and maintain a Ryerson e-mail account for timely communications between the instructor and the students;
2. Any changes in the course outline, test dates, marking or evaluation will be discussed in class prior to being implemented;
3. Assignments, projects, reports and other deadline-bound course assessment components handed in past the due date will receive a mark of ZERO, unless otherwise stated. Marking information will be made available at the time when such course assessment components are announced.
4. If you have taken the course previously and are currently looking to get a laboratory exemption, then you must fill out this form: http://www.ee.ryerson.ca/ guides/ECE-LabExemptionForm.pdf
5. Refer to our Departmental FAQ page for information on common questions and issues at the following link: https://www.ee.ryerson.ca/guides/Student.Academic.FAQ.html.
Missed Classes and/or Evaluations

When possible, students are required to inform their instructors of any situation which arises during the semester which may have an adverse effect upon their academic performance, and must request any consideration and accommodation according to the relevant policies as far in advance as possible. Failure to do so may jeopardize any academic appeals.

1. **Health certificates** - If a student misses the deadline for submitting an assignment, or the date of an exam or other evaluation component for health reasons, they should notify their instructor as soon as possible, and submit a Ryerson Student Health Certificate AND an Academic Consideration Request form within 3 working days of the missed date. Both documents are available at [https://www.ryerson.ca/senate/forms/medical.pdf](https://www.ryerson.ca/senate/forms/medical.pdf). If you are a full-time or part-time degree student, then you submit your forms to your own program department or school.

2. **Religious, Aboriginal and Spiritual observance** - If a student needs accommodation because of religious, Aboriginal or spiritual observance, they must submit a Request for Accommodation of Student Religious, Aboriginal and Spiritual Observance AND an Academic Consideration Request form within the first 2 weeks of the class or, for a final examination, within 2 weeks of the posting of the examination schedule. If the requested absence occurs within the first 2 weeks of classes, or the dates are not known well in advance as they are linked to other conditions, these forms should be submitted with as much lead time as possible in advance of the absence. Both documents are available at [www.ryerson.ca/senate/forms/relobservforminstr.pdf](www.ryerson.ca/senate/forms/relobservforminstr.pdf). If you are a full-time or part-time degree student, then you submit the forms to your own program department or school.

3. **Academic Accommodation Support** - Before the first graded work is due, students registered with the Academic Accommodation Support office (AAS - [www.ryerson.ca/studentlearningsupport/academic-accommodation-support](www.ryerson.ca/studentlearningsupport/academic-accommodation-support)) should provide their instructors with an Academic Accommodation letter that describes their academic accommodation plan.

Academic Integrity

Ryerson’s Policy 60 (the Academic Integrity policy) applies to all students at the University. Forms of academic misconduct include plagiarism, cheating, supplying false information to the University, and other acts. The most common form of academic misconduct is plagiarism - a serious academic offence, with potentially severe penalties and other consequences. It is expected, therefore, that all examinations and work submitted for evaluation and course credit will be the product of each student’s individual effort (or an authorized group of students). Submitting the same work for credit to more than one course, without instructor approval, can also be considered a form of plagiarism.

Suspicious of academic misconduct may be referred to the Academic Integrity Office (AIO). Students who are found to have committed academic misconduct will have a Disciplinary Notation (DN) placed on their academic record (not on their transcript) and will normally be assigned one or more of the following penalties:

1. A grade reduction for the work, ranging up to an including a zero on the work (minimum penalty for graduate work is a zero on the work);
2. A grade reduction in the course greater than a zero on the work. (Note that this penalty can only be applied to course components worth 10% or less, and any additional penalty cannot exceed 10% of the final course grade. Students must be given prior notice that such a penalty will be assigned (e.g. in the course outline or on the assignment handout);
3. An F in the course;
4. More serious penalties up to and including expulsion from the University.

The unauthorized use of intellectual property of others, including your professor, for distribution, sale, or profit is expressly prohibited, in accordance with Policy 60 (Sections 2.8 and 2.10). Intellectual property includes, but is not limited to:

1. Slides
2. Lecture notes
3. Presentation materials used in and outside of class
4. Lab manuals
5. Course packs
6. Exams

For more detailed information on these issues, please refer to the [Academic Integrity policy](https://www.ryerson.ca/senate/policies/pol60.pdf) and to the Academic Integrity Office website ([https://www.ryerson.ca/academicintegrity/](https://www.ryerson.ca/academicintegrity/)).

Important Resources Available at Ryerson

1. [The Library](https://library.ryerson.ca/) provides research workshops and individual assistance. Inquire at the Reference Desk on the second floor of the library, or go to library.ryerson.ca/guides/workshops.
2. [Student Learning Support](https://www.ryerson.ca/studentlearningsupport) offers group-based and individual help with writing, math, study skills and transition support, and other issues.

Approved by: _______________________________                Date ________________________________

Course Instructor

Approved by: _______________________________                Date ________________________________
Associate Chair or Program Director