Ryerson University

Department of Electrical, Computer, & Biomedical Engineering
Faculty of Engineering & Architectural Science

Course Outline (F2019)

COE758: Digital Systems Engineering

Instructor(s)	Lev Kirischian [Coordinator] Office: ENG432 Phone: (416) 979-5000 x 6076 Email: lkirisch@ryerson.ca Office Hours: TBA
Calendar Description	The emphasis of this course is an understanding of the system architecture around the processor. Course covers all types of modern semiconductor memory, cache and virtual memory organization, hard disk drives and video-output subsystem. Course gives classification of buses and description of concepts of bus organization, bus protocols, arbitration mechanisms and the concept of Direct Memory Access (DMA). The laboratory projects include design of Cache Controller and VGA-signal generator using VHDL in Xilinx CAD environment.
Prerequisites	(COE 538 or ELE 538) and COE 608
Antirequisites	None
Corerequisites	None
Compulsory Text(s):	1. David Patterson and John Hennessy, "Computer Organization and Design: The hardware /Software Interface", 5-rd edition, Morgan Kaufmann Publishers Inc., San Francisco, CA USA, ISBN-9780124077263
Reference Text(s):	1. Vincent Heuring and Harry Jordan, "Computer Systems Design and Architecture", Second edition, Prentice Hall, Pearson Education Inc., NJ, 07458, ISBN 0-13-048440-7 2. www.ee.ryerson.ca/~courses/ele758
Learning Objectives (Indicators)	At the end of this course, the successful student will be able to: 1. Understand the concepts of memory hierarchy organization and be able to apply this knowledge for the design of major architectural components of modern computer systems: cache memory, cache and main memory controllers, virtual memory elements and associated hardware/software drivers. Describe principles of interfacing the processor with different types of Input / Output (I/O) devices, estimate bus bandwidth, select the most effective bus organization and design I/O device controllers & adapters for modern computer systems. (**4a**) 2. Describe principles of interfacing the processor with different types of Input / Output (I/O) devices, estimate bus bandwidth, select the most effective bus organization and design I/O device controllers & adapters for modern computer systems. Learn modern integrated CAD tools (e.g. Xilinx ISE) and Hardware Description Languages (e.g. VHDL) and apply the principles of on-chip hardware design: including symbol creation, top-bottom design, high-level synthesis of IP-core architecture for designing the on-chip (FPGA-based) IP-cores for cache controllers, main memory interfaces, I/O device controllers and interfaces to real-time peripheral devices. (**4b**) 3. Integrate the on-chip (FPGA-based) IP-cores with the host computer and real-time peripheral device (e.g. SVGA video-display) and adjust timing parameters of the designed on-chip device controller. (**4c**) 4. Utilize the on-chip debugging techniques for modern FPGA-based hardware platforms (e.g. Xilinx Spartan FPGA devices), including synthesis and application of the on-chip test-vector generators, utilization of on-chip logic analyzers (e.g. Xilinx ChipScope), creation of the hardware emulation environment and systematic analysis of timing diagrams received from the on-chip logic analyzers. (**5a**) 5. Produce project reports using appropriate format of technical reports, grammar, and citation styles for technical and non-technical audiences. (**7a**) 6. Illustrate concepts including the structure of IP-cores VHDL-code with appropriate comments and obtained experimental results. (**7c**) **NOTE:** *Numbers in parentheses refer to the graduate attributes required by the Canadian Engineering Accreditation Board (CEAB).*
Course Organization	3.0 hours of lecture per week for 13 weeks 2.0 hours of lab/tutorial per week for 12 weeks

Teaching Assistants	TBA
Course Evaluation	

Theory	
Midterm Exam	25 %
Final Exam	45 %
Laboratory	
Lab Project 1	15 %
Lab Project 2	15 %
TOTAL:	100 %

Note: In order for a student to pass a course with **"Theory and Laboratory"** components, in addition to earning a minimum overall course mark of 50%, the student must pass the Laboratory and Theory portions separately by achieving a minimum of 50% in the combined Laboratory components and 50% in the combined Theory components. Please refer to the **"Course Evaluation"** section for details on the Theory and Laboratory components.

Examinations	Midterm exam in Week 7, two hours, closed book, problem solving (covers Weeks 1-6). Final exam, during exam period, three hours, closed-book, problem solving (covers all course material).
Other Evaluation Information	The laboratory projects include design of IP-cores of custom on-chip modules for cache controller and video-signal generator for SVGA-monitor. Both projects include all major stages of on-chip design of custom digital systems: coding on VHDL hardware description language, compilation and design evaluation in Xilinx ISE CAD environment and hardware implementation on Xilinx Spartan FPGA platform. In assigned projects students are required to develop the custom IP-cores on the base of Xilinx Spartan FPGA development platform. The goal is to apply the theoretical knowledge to on-chip system design and get practical experience in VHDL-coding, simulation and on-chip verification of the designed module. There are two projects associated with different aspects of the system-on-chip (SoC) design: i) IP-core design of the control-dominated circuit (Project 1: Cache Controller) and ii) IP-core design of the data-path dominated circuit (Project 2: Video-signal generator). For both projects the requirements are to demonstrate ability to write the VHDL-code, compile and simulate it in Xilinx ISE CAD environment, verify the behaviour on the Xilinx Spartan FPGA development platform using on-chip instrumentation (Chip-Scope), demonstrate the complete IP-core performance and submit the project report. Additionally, Project 2 requires integration the FPGA platform with the real-time I/O device (SVGA video-monitor) and demonstrate working project in all modes of operation. Lab Management The Lab Projects accounts for 15% each of the final mark. Each project must be demonstrated during the demonstration week. The project report must be submitted after successful project demonstration before the end of the demonstration week. The detailed evaluation of each project is as follows: 5% - Completed tutorials 7.5% - Symbol & block diagram design 7.5% - Compiled VHDL code demonstration 40% - Complete project demonstration on FPGA platform 40% - Project report Total 100% = 15% of the final mark All the tutorials and projects could be done individually or in group of 2 students. Equipment should not be moved before during or after the lab. In case if equipment seems to be defective it is a requirement to report to the lab instructor / technician who will take care of the problem.
Other Information	None

Course Content

Week	Hours	Chapters / Section	Topic, description
1	3	7 / 7.1	Introduction to COE 758: Scope and Objectives Management. 1. The basic structure of Memory hierarchy 2. Types of memory elements and their organization
2	3	7 / 7.1	Types of electronic memory and their organization: 1. Static and Dynamic Random Access Memory (RAM) structure and timing 2. Main memory component basis: DRAM EDO-DRAM SDRAM DDR-SDRAM RDRAM: structure interface and timing
3	3		Cache memory organization: 1. Principles of locality concepts terminology and organization of cache 2. Direct mapped cache: principles of operation and cache performance 3. Handling cache misses and writes. Cache & main memory coherence. (Chapter 7 Section 7.2)
4	3		Associative cache memory organization: 1. Ping-pong effect in direct mapped cache and cache efficiency 2. Two-way associative cache memory organization and operation 3. N-way associative cache: principles of operation pros and cons 4. Multi-level cache: concept organization and performance. (Chapter 7 Section 7.3)
5	3	7 / 7.4	Virtual memory: concept and organization: 1. Concept of memory virtualization terminology and general organization 2. Address translation page table and page replacement mechanism.
6	3		Virtual memory: concept and organization: 1. Fast address translation in Translation Look aside Buffer (TLB) 2. Integrating virtual memory: TLB cache main memory and secondary data storages (e.g. hard disc drive(s) solid state drive(s) etc.). (Chapter 7 Section 7.5)
7	2	7 / 7.1 - 7.5	Midterm test
8	3	8 / 8.1	Input-Output (I/O) subsystem organization: 1. Typical set of I/O devices in computing system 2. Interfacing processor(s) to I/O devices

9	3		Secondary data-storage devices: 1. Hard Disc Drive (HDD) principles of operation and performance 2. Solid State Drive (SSD) principles of operation and performance. (Chapter 8 Sections 8.1-8.2)
10	3	8 / 8.1 - 8.2	Video-output subsystem organization: 1. Video-displays: principles of operation in graphical and character modes 2. Video-adapters and video-processors: principles of operation and timing.
11	3	8 / 8.4	Buses: 1. Classification of buses synchronization and handshaking 2. Synchronous and asynchronous buses. Bus protocols and timing 3. Bus bandwidth calculation and methods for acceleration.
12	3	8 / 8.4	Bus arbitration and multi-level buses: 1. Bus arbitration mechanisms: Daisy-chain and centralized arbitration 2. Multi-level buses: Integration the memory bus and I/O buses 3. Direct memory Access (DMA): principles of operation and transfer modes.
13	2	8 / 8.5	Interaction between CPU I/O devices and memory: 1. Giving commands to I/O devices 2. Interrupt priority levels and interrupt service routines 3. Process of data transferring between CPU memory and I/O device.
13	1		Review and Catch-up

Laboratory/Tutorials/Activity Schedule

Week	Lab	Description
2	ENG409	Introduction to Xilinx ISE CAD and FPGA development environment
3	ENG409	Tutorials: Design components in Xilinx Spartan FPGA. Project 1 Specification
4-5	ENG409	VHDL-coding and compilation. Creation of simulation environment and verification
6	ENG409	Hardware emulation on FPGA platform and performance analysis with ChipScope
7	ENG409	Complete project 1 demonstration and report submission
8	ENG409	Introduction to video-processing systems and Project 2 specification
9	ENG409	VHDL-coding and compilation. Creation of simulation environment and verification
10	ENG409	Hardware emulation on FPGA platform and performance analysis with ChipScope
11	ENG409	Hardware integration with SVGA display and adjustment of timing.
12	ENG409	Complete project 2 demonstration and report submission

Policies & Important Information:

1. Students are required to obtain and maintain a Ryerson e-mail account for timely communications between the instructor and the students;
2. Any changes in the course outline, test dates, marking or evaluation will be discussed in class prior to being implemented;
3. Assignments, projects, reports and other deadline-bound course assessment components handed in past the due date will receive a mark of ZERO, unless otherwise stated. Marking information will be made available at the time when such course assessment components are announced.
4. Refer to our **Departmental FAQ** page for information on common questions and issues at the following link: https://www.ee.ryerson.ca/guides/Student.Academic.FAQ.html.

Missed Classes and/or Evaluations

When possible, students are required to inform their instructors of any situation which arises during the semester which may have an adverse effect upon their academic performance, and must request any consideration and accommodation according to the relevant policies as far in advance as possible. Failure to do so may jeopardize any academic appeals.

1. ***Health certificates*** - If a student misses the deadline for submitting an assignment, or the date of an exam or other evaluation component for health reasons, they should notify their instructor as soon as possible, and submit a Ryerson Student Health Certificate AND an Academic Consideration Request form within 3 working days of the missed date. Both documents are available at https://www.ryerson.ca/senate/forms/medical.pdf.. **If you are a full-time or part-time degree student, then you submit your forms to your own program department or school;**
2. ***Religious, Aboriginal and Spiritual observance*** - If a student needs accommodation because of religious, Aboriginal or spiritual observance, they must submit a Request for Accommodation of Student Religious, Aboriginal and Spiritual Observance AND an Academic Consideration Request form within the first 2 weeks of the class or, for a final examination, within 2 weeks of the posting of the examination schedule. If the requested absence occurs within the first 2 weeks of classes, or the dates are not known well in advance as they are linked to other conditions, these forms should be submitted with as much lead time as possible in advance of the absence. Both documents are available at www.ryerson.ca/senate/forms/relobservforminstr.pdf. **If you are a full-time or part-time degree student, then you submit the forms to your own program department or school;**
3. ***Academic Accommodation Support*** - Before the first graded work is due, students registered with theAcademic Accommodation Support office (AAS - www.ryerson.ca/studentlearningsupport/academic-accommodation-support) should provide their instructors with an Academic Accommodation letter that describes their academic accommodation plan.

Academic Integrity

Ryerson's Policy 60 (the Academic Integrity policy) applies to all students at the University. Forms of academic misconduct include plagiarism, cheating, supplying false information to the University, and other acts. The most common form of academic misconduct is plagiarism - a serious academic offence, with potentially severe penalties and other consequences. It is expected, therefore, that all examinations and work submitted for evaluation and course credit will be the product of each student's individual effort (or an authorized group of students). Submitting the same work for credit to more than one course, without instructor approval, can also be considered a form of plagiarism.

Suspicions of academic misconduct may be referred to the Academic Integrity Office (AIO). Students who are found to have committed academic misconduct will have a Disciplinary Notation (DN) placed on their academic record (not on their transcript) and will normally be assigned one or more of the following penalties:

1. A grade reduction for the work, ranging up to an including a zero on the work (minimum penalty for graduate work is a zero on the work);
2. A grade reduction in the course greater than a zero on the work. (Note that this penalty can only be applied to course components worth 10% or less, and any additional penalty cannot exceed 10% of the final course grade. Students must be given prior notice that such a penalty will be assigned (e.g. in the course outline or on the assignment handout);
3. An F in the course;
4. More serious penalties up to and including expulsion from the University.

The unauthorized use of intellectual property of others, including your professor, for distribution, sale, or profit is expressly prohibited, in accordance with Policy 60 (Sections 2.8 and 2.10). Intellectual property includes, but is not limited to:

1. Slides
2. Lecture notes
3. Presentation materials used in and outside of class
4. Lab manuals
5. Course packs
6. Exams

For more detailed information on these issues, please refer to theAcademic Integrity policy(https://www.ryerson.ca/senate/policies/pol60.pdf) and to the Academic Integrity Office website (https://www.ryerson.ca/academicintegrity/).

Important Resources Available at Ryerson

1. The Library (https://library.ryerson.ca/) provides research workshops and individual assistance. Inquire at the Reference Desk on the second floor of the library, or go to library.ryerson.ca/guides/workshops
2. Student Learning Support(https://www.ryerson.ca/studentlearningsupport) offers group-based and individual help with writing, math, study skills and transition support, and other issues.