Ryerson University

Department of Electrical & Computer Engineering
Faculty of Engineering & Architectural Science

Course Outline (WINTER 2017)

COE 838: Systems-on-Chip Design

Instructor	NAME: Gul N. Khan Office: ENG 448 Phone: 416-979-5000 ext: 6084 E-mail: gnkhan@ryerson.ca, gnkhan@ee.ryerson.ca Office Hours: Tuesday 12:15-1:30PM
Calendar Description	This course will cover the basics of system-on-chip (SoC) design, hardware-software co-specification, co-synthesis and network-on-chip (NoC) systems. It provides the advance knowledge required for system-on-chip design, multi-core architectures and embedded systems on a chip. Students will also be introduced to the main principles of SoC modeling and design using SystemC. Various soft processor cores such as Nios-II and other IPs will be explored. Interconnection structures such as AMBA, Avalon and IBM Core-connect for SoC design will be covered in detail. Various SoC development tools will be utilized in the labs and projects.
Prerequisites	*COE538; COE718 or ELE734*
Compulsory Text(s):	1. *Michael J. Flynn, Wayne Luk*, Computer System Design: System on Chip, John Wiley and Sons Inc. 2011, ISBN 978-0-470-64336-5 2. *D.C. Black, J Donovan, B. Bunton, A. Keist*, SystemC: From the Ground Up, 2nd Edition, Springer 2010, ISBN 978-0-387-69958-5
Reference Text(s)	3. *M. Wolf*, Computer as Components: Principles of Embedded Computing System Design, 3rd or 4th Edition, Morgan Kaufman Publishers 2016, ISBN 978-0-12-805387-4 Some relevant review articles to be identified by the instructor and will be available at the course web page.
Learning Objectives (Indicators)	At the end of this course, the successful student will be able to: 1. Interconnect engineering concepts related to soft-processor cores, hardware and software systems to design an SoC for real-world applications. Learn to employ specialized knowledge of subsystems like processor cores and other SoC components to design an embedded SoC. (1c) and (1d) **Assessment Methods:** Final/Midtern examination question, some Labs and the project. 2. Improve students' capabilities of using the technical knowledge of processor architecture, peripherals, programming, and CAD tools to design application specific SoCs. Solve various challenges of high performance SoC design in multiple stages by employing hardware/software co-design methodologies to test and verify each stage and then integrate different stages into an efficient SoC architecture. (4a) and (4c) **Assessment Methods:** Labs, project and final examination question. 3. Learn and efficient use of different SoC simulation, modeling and prototyping tools including SystemC, QSys and Quartus-II. These tools facilitate co-simulation and co-design of SoCs. (5c) **Assessment Methods:** Labs, project and midterm examination question. 4. Demonstrate the main features of the course-project and answer critical and project specific questions during project demo and oral sessions. Write project report by following a standard IEEE like format, where all the lab and project

	reports are evaluated based on their completeness, English, and citations. (7a) and (7b). **Assessment Methods:** Labs and course project. **NOTE**: *Numbers in parentheses refer to the graduate attributes required by the Canadian Engineering Accreditation Board (CEAB).*
Course Organization	3 hours of lecture per week for 13 weeks, in 3 sections 1 hours of lab/tutorial per week for 12 weeks 3 Lab/tutorial sections of maximum 20 students 2 Teaching Assistants, 1-2 sections per TA
Teaching Assistants	Mr. Rishabh Kumar e-mail: r2kumar@ryerson.ca Mr. Alireza Pourali, e-mail: alireza.pourali@ryerson.ca
Course Evaluation	(The following is a Table and you can add/remove rows/columns as needed) Midterm Exam 30 % Labs with formal Reports 15 % Project 15 % Final Exam 30 % **TOTAL**: 100 %
Examinations	Midterm exam in Week 7, 1.5 hours, closed book (covers Weeks 1-6). Final exam, during exam period, two hours, closed-book (covers Weeks 1-13).
Other Evaluation and/or Information	There will be bonus (optional) project component carrying additional 3-5% marks.

Course Content

Lecture/Week	hours	Topic, description
1	3	Introduction to System on Chip (SoC) An SoC Design Approach
2	3	Introduction to SystemC Using SystemC for SoC Co-specification
3	3	SystemC based Modeling and Analysis of SoCs
4	3	Hardware-Software Cosynthesis and Accelerators based Embedded System Design
5	3	Basics of Chips and SoC ICs
6	3	SoPC (System on Programmable Chips) and SoC Design
7	3	SoC Soft Cores Processors **Mid-term Exam**
8	3	Various Soft CPU Cores: ARM-A9, OpenRISC, Leon4, OpenSPARC
9	3	SoC Interconnection - On-Chip Busses: AMBA, Core-connect, Avalon, etc.
10	3	NoC (Network on Chip) based Interconnection Regular (Mesh, Torus, Tree, etc.) and Application Specific NoC Topologies
11	3	Multi-core and MPSoC (Multiprocessor SoC) Architectures
12	3	SoC Application Case Studies (If time permits)
13	3	Catching up and Review

Laboratory/Project

Weeks	Title	Room
2	**Lab1:** SystemC: Introduction and Tutorial. http://www.doulos.com/knowhow/systemc/	ENG 412
3	**Lab 2a**: SystemC based Accelerator for SoC	"
4	**Lab 2b:** JPEG Encoder/Decoder SoC Design using SystemC	"
5	**Lab 3:** DE1-SoC Tutorial - Creating SoCs using FPGA and Hard A9 Processor Systems	"
6	Individual/Team **Course Project Selection**	"
7	**Lab4:** Designing and Interfacing Custom IP with an FPGA/HPS System	"
8	Summary: Project Approach (1-2 pages)	"
9		"
10	Demo of Project Progress and Interim (project) Report	"
11		"
12	Final Project Demonstration	"
13	Project Presentation and (Final) Report	"

Important Notes

1. All of the required course-specific written reports will be assessed not only on their technical/academic merit, but also on the communication skills exhibited through these reports.

2. All assignment and lab/tutorial reports must have the standard cover page which must be signed by the student(s) prior to submission of the work. Submissions without the cover page **will not** be accepted. The cover page can be found on the departmental web site: Standard Assignment/Lab Cover Page

3. Should a student miss a mid-term test or equivalent (e.g. studio or presentation), with appropriate documentation, a make-up assessment ***may*** be scheduled. Alternatively, the weight of the missed work is placed on the final exam, or another single assessment. This may not cause that exam or assessment to be worth more than 70% of the student's final grade. If a student misses a scheduled make-up test or exam, the grade may be distributed over other course assessments even if that makes the grade on the final exam worth more than 70% of the final grade in the course. Make-up assessments cover the same material as the original assessment but need not be of an identical format.

4. Students who miss a final exam for a verifiable reason and who cannot be given a make-up exam prior to the submission of final course grades, must be given a grade of INC (as outlined in the *Grading Promotion and Academic Standing Policy)* and a make-up exam (normally within 2 weeks of the beginning of the next semester) that carries the same weight and measures the same knowledge, must be scheduled.

5. Medical or Compassionate documents for the missing of an exam must be submitted within 3 working days of the exam. Students are responsible for notifying the instructor that they will be missing an exam as soon as possible.

6. **If a student is requesting accommodation due to a religious, aboriginal and/or spiritual observance, he or she must submit a Request for Accommodation of Student Religious, Aboriginal, and Spiritual Observance AND an Academic Consideration form within the FIRST TWO WEEKS OF CLASS or, for a final examination, within two weeks of the posting of the examination schedule**. If the required absence occurs within the first two weeks of classes, or the dates are not known well in advance as they are linked to other conditions, these forms should be submitted with as much lead time as possible in advance of the required absence.
   Both documents are available at http://www.ryerson.ca/senate/forms/relobservforminstr.pdf. Full-time or part-time degree students must submit the forms to their own program department or school.

7. The results of the first test or mid-term exam will be returned to students before the deadline to drop an undergraduate course in good Academic Standing.

8. Students are required to adhere to all relevant University policies including:

- Undergraduate Grading, Promotion and Academic Standing: http://www.ryerson.ca/senate/policies/pol46.pdf
- Student Code of Academic Conduct: http://www.ryerson.ca/senate/policies/pol60.pdf
- Student Code of Non-Academic Conduct: http://www.ryerson.ca/senate/policies/pol61.pdf
- Undergraduate Academic Consideration and Appeals: http://www.ryerson.ca/senate/policies/pol134.pdf
- Examination Policy: http://www.ryerson.ca/senate/policies/pol135.pdf
- Course Management Policy: http://www.ryerson.ca/senate/policies/pol145.pdf
- Accommodation of Student Religious, Aboriginal and Spiritual Observance: http://www.ryerson.ca/senate/policies/pol150.pdf
- Establishment of Student E-mail Accounts for Official University Communication: http://www.ryerson.ca/senate/policies/pol157.pdf

9. Students are required to obtain and maintain a Ryerson e-mail account for timely communications between the instructor and the students.

10. Any changes in the course outline, test dates, marking or evaluation will be discussed in class prior to being implemented.

11. Assignments, projects, reports and other deadline-bound course assessment components handed in past the due date will receive a mark of ZERO. Marking information will be made available at the time when such course assessment components are announced.

12. If you have taken the course previously and are currently looking to get a laboratory exemption, then you must fill out this form: http://www.ee.ryerson.ca/guides/ECE-LabExemptionForm.pdf

Approved by: _____ Date _____
Course Instructor

Approved by: _____ Date _____
Associate Chair or Program Director