# Course Outline (F2019)

**ELE734: Low Power Digital Integrated Circuits**

## Instructor(s)
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Office Hours: Wednesday 10am - 11:30am (May 22, 2019 - June 27, 2019)

## Calendar Description
This course deals with the design of Digital CMOS integrated circuits. The course consists of three essential components: Theory, Laboratory, and project. Variety of design techniques, such as Static CMOS, Dynamic CMOS, and Transmission Gate are discussed in theory. These designs are studied on basic logic gates as well as combinational and sequential circuits. The lessons learned are applied to arithmetic building blocks such as adders and decoders. A MOS transistor is studied using I-V equations, and the different areas of operations are modeled. The static (DC) are dynamic (transient) behaviors for an important building block, a CMOS inverter, are studied in depth.

## Prerequisites
ELE 504

## Antirequisites
None

## Corequisites
None

## Compulsory Text(s):
2. ELE734 Low Power Digital Integrated Circuits Laboratory Manual, by Adnan Kabbani and Tarek Khan

## Reference Text(s):
At the end of this course, the successful student will be able to:

1. Develop good understanding of the appropriate level of modeling used in VLSI design for area, performance and power optimization. (1c)
2. Use technical knowledge including CMOS layout, delay, and power estimation techniques to design reliable, high performance, and low power CMOS digital circuits and systems. Apply the CMOS digital circuit design principles to define an accurate CMOS design problem statement. Recognize that good problem definition assists the CMOS design process. (4a)
3. Apply the CMOS digital circuit design principles to define an accurate CMOS design problem statement. Recognize that good problem definition assists the CMOS design process. Describe differences between the various approaches that can be used to solve a CMOS digital circuit design problem. Select one specific approach to solve the problem. When the selected approach fails to solve the problem satisfactorily, analyze the cause of failure using the principles of CMOS digital circuit design. Based on the analysis, come up with new suggestions to improve the existing approach. Integrate the new suggestions into the existing design plan. Judge the completeness and quality of the generated solutions based on the principles of CMOS digital circuit design. (4b)
4. Use Cadence Tools to Implement CMOS digital circuit design and obtained experimental results. (5a)

**NOTE:** Numbers in parentheses refer to the graduate attributes required by the Canadian Engineering Accreditation Board (CEAB).

## Course Organization
3.0 hours of lecture per week for 13 weeks
2.0 hours of lab/tutorial per week for 12 weeks

## Teaching Assistants
TBA
### Course Evaluation

<table>
<thead>
<tr>
<th>Component</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Midterm Exam</td>
<td>25 %</td>
</tr>
<tr>
<td>Lab 1</td>
<td>10 %</td>
</tr>
<tr>
<td>Lab 2</td>
<td>7 %</td>
</tr>
<tr>
<td>Lab 3</td>
<td>10 %</td>
</tr>
<tr>
<td>Lab 4</td>
<td>8 %</td>
</tr>
<tr>
<td>Final Exam</td>
<td>40 %</td>
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<tr>
<td><strong>TOTAL:</strong></td>
<td><strong>100 %</strong></td>
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</tbody>
</table>

**Note:** In order for a student to pass a course with "Theory and Laboratory" components, in addition to earning a minimum overall course mark of 50%, the student must pass the Laboratory and Theory portions separately by achieving a minimum of 50% in the combined Laboratory components and 50% in the combined Theory components. Please refer to the "Course Evaluation" section for details on the Theory and Laboratory components.

### Examinations

- Midterm exam in Week 8, 1.5 hours, closed book (covers Weeks 1-6 of lecture and laboratory material).
- Final exam, during exam period, 3 hours, closed book (covers all the course material).

### Other Evaluation Information

- The mid-term test and final examination will be closed book.
- In order to achieve a passing grade in this course, the student must achieve an average of at least 50% in both theoretical and laboratory components.
- The written reports will be assessed not only on their technical or academic merit, but also on the communication skills of the author as exhibited through the reports.

### Other Information

None

### Course Content

<table>
<thead>
<tr>
<th>Week</th>
<th>Hours</th>
<th>Chapters / Section</th>
<th>Topic, description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>3</td>
<td>Introduction to CMOS (Chapter 1 Sections 1.1-1.12)</td>
<td></td>
</tr>
<tr>
<td>2-3</td>
<td>6</td>
<td>MOS Transistor Theory (Chapter 2 Sections 2.1-2.6)</td>
<td></td>
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<tr>
<td>4-5</td>
<td>6</td>
<td>Delay (Chapter 4 Sections 4.1-4.8)</td>
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<tr>
<td>6-7</td>
<td>6</td>
<td>Power (Chapter 5 Sections 5.1-5.6)</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>3</td>
<td>Interconnect (Chapter 6 Sections 6.1-6.5)</td>
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</tbody>
</table>
### Circuit Simulation
(Chapter 8 Sections 8.1-8.7)

### Combinational Circuit Design
(Chapter 9 Sections 9.1-9.7)

### Sequential Circuit Design
(Chapter 10 Sections 10.1-10.8)

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### Laboratory/Tutorials/Activity Schedule

<table>
<thead>
<tr>
<th>Week</th>
<th>Lab</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-4</td>
<td>ENG412</td>
<td>Characteristics of MOSFET Devices</td>
</tr>
<tr>
<td>5-6</td>
<td>ENG412</td>
<td>CMOS Inverter Design</td>
</tr>
<tr>
<td>7-10</td>
<td>ENG412</td>
<td>CMOS Logic Families</td>
</tr>
<tr>
<td>11-13</td>
<td>ENG412</td>
<td>1-bit CMOS Full Adder</td>
</tr>
</tbody>
</table>

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### Policies & Important Information:

1. Students are required to obtain and maintain a Ryerson e-mail account for timely communications between the instructor and the students;
2. Any changes in the course outline, test dates, marking or evaluation will be discussed in class prior to being implemented;
3. Assignments, projects, reports and other deadline-bound course assessment components handed in past the due date will receive a mark of ZERO, unless otherwise stated. Marking information will be made available at the time when such course assessment components are announced.
4. Refer to our [Departmental FAQ](https://www.ee.ryerson.ca/guides/Student.Academic.FAQ.html) page for information on common questions and issues at the following link:

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### Missed Classes and/or Evaluations

When possible, students are required to inform their instructors of any situation which arises during the semester which may have an adverse effect upon their academic performance, and must request any consideration and accommodation according to the relevant policies as far in advance as possible. Failure to do so may jeopardize any academic appeals.

1. **Health certificates** - If a student misses the deadline for submitting an assignment, or the date of an exam or other evaluation component for health reasons, they should notify their instructor as soon as possible, and submit a Ryerson Student Health Certificate AND an Academic Consideration Request form within 3 working days of the missed date. Both documents are available at [https://www.ryerson.ca/senate/forms/medical.pdf](https://www.ryerson.ca/senate/forms/medical.pdf). If you are a full-time or part-time degree student, then you submit your forms to your own program department or school;
2. **Religious, Aboriginal and Spiritual observance** - If a student needs accommodation because of religious, Aboriginal or spiritual observance, they must submit a Request for Accommodation of Student Religious, Aboriginal and Spiritual Observance AND an Academic Consideration Request form within the first 2 weeks of the class or, for a final examination, within 2 weeks of the posting of the examination schedule. If the requested absence occurs within the first 2 weeks of classes, or the dates are not known well in advance as they are linked to other conditions, these forms should be submitted with as much lead time as possible in advance of the absence. Both documents are available at [www.ryerson.ca/senate/forms/relobservforminstr.pdf](http://www.ryerson.ca/senate/forms/relobservforminstr.pdf). If you are a full-time or part-time degree student, then you submit the forms to your own program department or school;
3. **Academic Accommodation Support** - Before the first graded work is due, students registered with the [Academic Accommodation Support office](https://www.ryerson.ca/studentlearningsupport/academic-accommodation-support) should provide their instructors with an Academic Accommodation letter that describes their academic accommodation plan.

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### Academic Integrity

Ryerson’s [Policy 60 (the Academic Integrity policy)](https://www.ryerson.ca/policies/60) applies to all students at the University. Forms of academic misconduct include plagiarism, cheating, supplying false information to the University, and other acts. The most common form of academic misconduct is plagiarism - a serious academic offence,
with potentially severe penalties and other consequences. It is expected, therefore, that all examinations and work submitted for evaluation and course credit will be the product of each student's individual effort (or an authorized group of students). Submitting the same work for credit to more than one course, without instructor approval, can also be considered a form of plagiarism.

Suspicious of academic misconduct may be referred to the Academic Integrity Office (AIO). Students who are found to have committed academic misconduct will have a Disciplinary Notation (DN) placed on their academic record (not on their transcript) and will normally be assigned one or more of the following penalties:

1. A grade reduction for the work, ranging up to an including a zero on the work (minimum penalty for graduate work is a zero on the work);
2. A grade reduction in the course greater than a zero on the work. (Note that this penalty can only be applied to course components worth 10% or less, and any additional penalty cannot exceed 10% of the final course grade. Students must be given prior notice that such a penalty will be assigned (e.g. in the course outline or on the assignment handout);
3. An F in the course;
4. More serious penalties up to and including expulsion from the University.

The unauthorized use of intellectual property of others, including your professor, for distribution, sale, or profit is expressly prohibited, in accordance with Policy 60 (Sections 2.8 and 2.10). Intellectual property includes, but is not limited to:

1. Slides
2. Lecture notes
3. Presentation materials used in and outside of class
4. Lab manuals
5. Course packs
6. Exams

For more detailed information on these issues, please refer to the Academic Integrity policy (https://www.ryerson.ca/senate/policies/pol60.pdf) and to the Academic Integrity Office website (https://www.ryerson.ca/academicintegrity/).

Important Resources Available at Ryerson

1. The Library (https://library.ryerson.ca/) provides research workshops and individual assistance. Inquire at the Reference Desk on the second floor of the library, or go to library.ryerson.ca/guides/workshops
2. Student Learning Support (https://www.ryerson.ca/studentlearningsupport) offers group-based and individual help with writing, math, study skills and transition support, and other issues.