## Course Outline (W2020)

### ELE863: VLSI Circuits for Data Communications

#### Instructor(s)

Fei Yuan [Coordinator]
Office: ENG 433  
Phone: (416) 979-5000 x 6100  
Email: fyuan@ryerson.ca  
Office Hours: Mon.12-2 pm., Wed.10-12

#### Calendar Description

An advanced course on design of VLSI circuits for data communications over wire channels. The theoretical component consists of: switching noise and grounding of mixed analog-digital circuits, modeling of wire channels, clock generation and distribution, power distribution on chip, ESD protection, channel equalization, clock and data recovery. The laboratory component consists of design of clock and data recovery circuits using state-of-the-art CMOS technology and CAD tools.

#### Prerequisites

ELE 704 or ELE 734

#### Antirequisites

None

#### Corerequisites

None

#### Compulsory Text(s):

1. ELE 863 Lecture Notes from Dr. Fei Yuan (available from D2L).
2. Laboratory manual: ELE 863 Laboratory Manual (available from D2L).

#### Reference Text(s):

6. Published peer-reviewed scientific papers in scientific journals and conference proceedings.

#### Learning Objectives (Indicators)

At the end of this course, the successful student will be able to:

1. Improve their capabilities of using the technical knowledge of VLSI circuits to design a transceiver for data communications. (4b)
2. Utilize computer-aided design tools for integrated circuit design to iteratively design a transceiver for data communications over wire channels. (4c)
3. Proficiency in use of computer-aided design tools from Cadence Design Systems for integrated circuit design to design and analyze a transceiver for data communications over wire channels. (5a)
4. Write professionally prepared laboratory reports. Laboratory reports are evaluated on their correctness, completeness, English, and quality of graphics. (7a), (7c)

**NOTE:** Numbers in parentheses refer to the graduate attributes required by the Canadian Engineering Accreditation Board (CEAB).

#### Course Organization

3.0 hours of lecture per week for 13 weeks  
2.0 hours of lab/tutorial per week for 12 weeks

#### Teaching Assistants

Parth Parekh, Email: parth.parekh@ryerson.ca
Course Evaluation

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Midterm Exam</td>
<td>30 %</td>
<td></td>
</tr>
<tr>
<td>Lab Projects</td>
<td>30 %</td>
<td></td>
</tr>
<tr>
<td>Final Exam</td>
<td>40 %</td>
<td></td>
</tr>
<tr>
<td>TOTAL:</td>
<td>100 %</td>
<td></td>
</tr>
</tbody>
</table>

**Note:** In order for a student to pass a course with “Theory and Laboratory” components, in addition to earning a minimum overall course mark of 50%, the student must pass the Laboratory and Theory portions separately by achieving a minimum of 50% in the combined Laboratory components and 50% in the combined Theory components. Please refer to the “Course Evaluation” section for details on the Theory and Laboratory components.

Examinations

1. 2-hour closed-book midterm exam during regular lecture time with date to be determined in class.
2. 3-hour closed-book final exam during university exam period.

Other Evaluation Information
None

Other Information
None

Course Content

<table>
<thead>
<tr>
<th>Week</th>
<th>Hours</th>
<th>Chapters / Section</th>
<th>Topic, description</th>
</tr>
</thead>
</table>
| 1-2  | 6     | Module 1 - Modeling of wire channels  
|      |       | 1) Resistance capacitance and inductance of wire channels  
|      |       | 2) Lumped models of wire channels  
|      |       | 3) Distributed models of wire channels  
|      |       | 4) Transmission-line models of wire channels  
|      |       | (Chapter 1) |
| 3    | 3     | Module 2 - Electrical signaling  
|      |       | 1) Single-ended signaling  
|      |       | 2) Fully differential signaling  
|      |       | 3) Pseudo-differential signaling  
|      |       | 4) Low-voltage differential signaling (LVDS)  
|      |       | 5) Voltage-mode signaling versus current-mode signaling  
|      |       | Incremental signaling  
|      |       | (Chapter 2) |
| 4    | 3     | Module 3 - Fundamentals of serial links  
|      |       | 1) Pulse amplitude modulation (PAM)  
|      |       | 2) Pulse width modulation (PWM)  
|      |       | 3) Eye diagrams  
|      |       | 4) Inter-symbol interference (ISI)  
|      |       | 5) Bit-error rate  
|      |       | 6) Test of serial links  
|      |       | (Chapter 3) |
| 5-7  | 9   | Module 4 – Phase/Frequency-locked loops (PLLs/FLLs)  
|      |     | 1) Phase-lock loops in serial links  
|      |     | 2) Voltage-controlled ring oscillators  
|      |     | 3) Spectrum of voltage-controlled oscillators  
|      |     | 4) Phase detectors  
|      |     | 5) Charge pumps  
|      |     | 6) Loop dynamics of phase-locked loops  

| 8-10 | 9   | Module 5 - Pre-emphasis  
|      |     | 1) Channel equalization  
|      |     | 2) Pre-emphasis strategies  
|      |     | 3) Basic idea of pre-emphasis  
|      |     | 4) Pre-emphasis algorithms  
|      |     | 5) Pre-emphasis algorithms: A zero/pole perspective  
|      |     | 6) Pre-emphasis algorithms: A frequency response perspective  
|      |     | 7) Pre-emphasis waveforms  
|      |     | 8) Implementation of pre-emphasis FIR filters  
|      |     | 9) Advantages of pre-emphasis  
|      |     | 10) Limitations of pre-emphasis  

| 11-12 | 6   | Module 6 - Continuous-time linear equalization  
|       |     | 1) Channel impairments  
|       |     | 2) Channel equalization  
|       |     | 3) Continuous-time linear equalization  
|       |     | 4) Continuous-time linear equalization: Source degeneration  
|       |     | 5) Continuous-time linear equalization: Negative capacitors  
|       |     | 6) Continuous-time linear equalization: Inductor shunt-peaking  
|       |     | 7) Continuous-time linear equalization: Complete design  

|       |     | Module 7 - Decision feedback equalization  
|       |     | 1) Background  
|       |     | 2) Channel equalization  
|       |     | 3) Pre-emphasis  
|       |     | 4) Decision feedback equalization  
|       |     | 5) Loop unrolling  
|       |     | 6) Half-rate direct feedback  
|       |     | 7) Tap summation  
|       |     | 8) DFE: State-of-the-art  
|       |     | 9) Adaptive DFE  
|       |     | 10) Adaptive data-DFE  
|       |     | 11) Adaptive EOM-DFE  
|       |     | 12) Adaptive edge-DFE  

|       |     | Module 8 - Clock and data recovery  
|       |     | 1) Clock recovery  
|       |     | 2) Frequency drift of receiver PLL  
|       |     | 3) Direct coupling and AC coupling  
|       |     | 4) Data encoding  
|       |     | 5) Classification of clock recovery  
|       |     | 6) Clock recovery using phase tracking  
|       |     | 7) Clock recovery using phase picking  
|       |     | 8) Clock recovery using phase interpolation  

Laboratory/Tutorials/Activity Schedule
### Week | Lab | Description
--- | --- | ---
2-3 | ENG412 | Laboratory Design Project 1: Wire channels
4-5 | ENG412 | Laboratory Design Project 2: Continuous-time linear equalizers
6-7 | ENG412 | Laboratory Design Project 3: Phase-locked loops
8-9 | ENG412 | Laboratory Design Project 4: Pre-emphasis
10-11 | ENG412 | Laboratory Design Project 5: Decision feedback equalizers
12-13 | ENG412 | Laboratory Design Project 6: Clock and data recovery

**Policies & Important Information:**

1. Students are required to obtain and maintain a Ryerson e-mail account for timely communications between the instructor and the students;
2. Any changes in the course outline, test dates, marking or evaluation will be discussed in class prior to being implemented;
3. Assignments, projects, reports and other deadline-bound course assessment components handed in past the due date will receive a mark of ZERO, unless otherwise stated. Marking information will be made available at the time when such course assessment components are announced.
4. Refer to our Departmental FAQ page for information on common questions and issues at the following link: [https://www.ee.ryerson.ca/guides/Student.Academic.FAQ.html](https://www.ee.ryerson.ca/guides/Student.Academic.FAQ.html).

**Missed Classes and/or Evaluations**

When possible, students are required to inform their instructors of any situation which arises during the semester which may have an adverse effect upon their academic performance, and must request any consideration and accommodation according to the relevant policies as far in advance as possible. Failure to do so may jeopardize any academic appeals.

1. **Health certificates** - If a student misses the deadline for submitting an assignment, or the date of an exam or other evaluation component for health reasons, they should notify their instructor as soon as possible, and submit a Ryerson Student Health Certificate AND an Academic Consideration Request form within 3 working days of the missed date. Both documents are available at [https://www.ryerson.ca/senate/forms/medical.pdf](https://www.ryerson.ca/senate/forms/medical.pdf). If you are a full-time or part-time degree student, then you submit your forms to your own program department or school;
2. **Religious, Aboriginal and Spiritual observance** - If a student needs accommodation because of religious, Aboriginal or spiritual observance, they must submit a Request for Accommodation of Student Religious, Aboriginal and Spiritual Observance AND an Academic Consideration Request form within the first 2 weeks of the class or, for a final examination, within 2 weeks of the posting of the examination schedule. If the requested absence occurs within the first 2 weeks of classes, or the dates are not known well in advance as they are linked to other conditions, these forms should be submitted with as much lead time as possible in advance of the absence. Both documents are available at [www.ryerson.ca/senate/forms/relobservforminstr.pdf](http://www.ryerson.ca/senate/forms/relobservforminstr.pdf). If you are a full-time or part-time degree student, then you submit the forms to your own program department or school;
3. **Academic Accommodation Support** - Before the first graded work is due, students registered with the Academic Accommodation Support office (AAS - www.ryerson.ca/studentlearningsupport/academic-accommodation-support) should provide their instructors with an Academic Accommodation letter that describes their academic accommodation plan.

**Academic Integrity**

Ryerson’s **Policy 60 (the Academic Integrity policy)** applies to all students at the University. Forms of academic misconduct include plagiarism, cheating, supplying false information to the University, and other acts. The most common form of academic misconduct is plagiarism - a serious academic offence, with potentially severe penalties and other consequences. It is expected, therefore, that all examinations and work submitted for evaluation and course credit will be the product of each student's individual effort (or an authorized group of students). Submitting the same work for credit to more than one course, without instructor approval, can also be considered a form of plagiarism.

Suspiscions of academic misconduct may be referred to the Academic Integrity Office (AIO). Students who are found to have committed academic
misconduct will have a Disciplinary Notation (DN) placed on their academic record (not on their transcript) and will normally be assigned one or more of the following penalties:

1. A grade reduction for the work, ranging up to an including a zero on the work (minimum penalty for graduate work is a zero on the work);
2. A grade reduction in the course greater than a zero on the work. (Note that this penalty can only be applied to course components worth 10% or less, and any additional penalty cannot exceed 10% of the final course grade. Students must be given prior notice that such a penalty will be assigned (e.g. in the course outline or on the assignment handout);
3. An F in the course;
4. More serious penalties up to and including expulsion from the University.

The unauthorized use of intellectual property of others, including your professor, for distribution, sale, or profit is expressly prohibited, in accordance with Policy 60 (Sections 2.8 and 2.10). Intellectual property includes, but is not limited to:

1. Slides
2. Lecture notes
3. Presentation materials used in and outside of class
4. Lab manuals
5. Course packs
6. Exams

For more detailed information on these issues, please refer to the Academic Integrity policy (https://www.ryerson.ca/senate/policies/pol60.pdf) and to the Academic Integrity Office website (https://www.ryerson.ca/academicintegrity/).

Important Resources Available at Ryerson

1. The Library (https://library.ryerson.ca/) provides research workshops and individual assistance. Inquire at the Reference Desk on the second floor of the library, or go to library.ryerson.ca/guides/workshops
2. Student Learning Support (https://www.ryerson.ca/studentlearningsupport) offers group-based and individual help with writing, math, study skills and transition support, and other issues.