Ryerson University

Department of Electrical & Computer Engineering
Faculty of Engineering & Architectural Science

Course Outline (W2017)

ELE863: VLSI Circuits for Data Communications

Instructor	NAME: Fei Yuan Office: ENG 433 Phone: 416-979-5000 ext: 6100 E-mail: fyuan@ryerson.ca Office Hours: Tue. 1-2 pm.
Calendar Description	An advanced course on design of VLSI circuits for data communications over wire channels. The theoretical component consists of: Modeling of wire channels, electrical signaling, phase-locked loops, channel equalization, and clock and data recovery. The laboratory design project deals with the design of a Gbps serial link using state-of-the-art CMOS technology and CAD tools.
Prerequisites	*ELE724 or ELE734*
Compulsory Text(s):	1. *ELE 863 Lecture Notes* from Dr. Fei Yuan (available from D2L). 2. Laboratory manual: *ELE 863 Laboratory Manual* (available from D2L).
Reference Text(s)	1. W. Dally and J. Poulton, *Digital Systems Engineering*, Cambridge University Press, 1998. 2. K. Oh and X. Yuan (ed.), *High-speed signaling: Jitter Modeling, Analysis, and Budgeting*, Prentice-Hall, 2012. 3. H. Johnson and M. Graham, *High-speed digital design - A handbook of black magic*, Prentice-Hall, 1993. 4. F. Yuan, *CMOS Current-Mode Circuits for Data Communicatio*ns. Springer, 2006. 5. F. Yuan (ed.), *CMOS Time-Mode Circuits and Systems: Principles and Applications*, CRC Press, 2015. 6. Stojanovic, *Channel-limited high-speed links: modeling, analysis and design*, PhD Dissertation, Stanford University, 2004. 7. Published peer-reviewed scientific papers in scientific journals and conference proceedings.
Learning Objectives (Indicators)	At the end of this course, the successful student will be able to: 1) Improve their capabilities of using the technical knowledge of semiconductor devices, ESD protection, memories, interconnects, switching noise and computer-aided design tools to design complex VLSI circuits for particular applications (***4d – Generate solutions***). Utilize computer-aided design tools for IC design to iteratively improve designed complex VLSI circuits to meet the design specifications of given applications (***4h - Iterations***). **Assessment Methods:** Mid-term and final examination papers. 2) Proficiency in use of computer-aided design tools from Cadence Design Systems for integrated circuit (IC) design to design and analyze complex VLSI circuits. (***5c – Use of engineering tools***)

	Assessment Methods: Laboratory design project reports. 3) Write professionally prepared laboratory reports and course project report in confirmation to IEEE format. Laboratory and project reports are evaluated on their correctness, completeness, English, and quality of graphics (***7a – Written, 7d - Graphical***) **Assessment Methods:** Professionally prepared laboratory design project reports. **NOTE**: *Numbers in parentheses refer to the graduate attributes required by the Canadian Engineering Accreditation Board (CEAB).*
Course Organization	3 hours of lecture per week for 13 weeks, 1 section. 2 hours of lab bi-weekly 1 Lab sections of maximum 22 students 1 Teaching Assistant, 1 section per TA
Teaching Assistants	(The following is a Table and you can add/remove rows/columns as needed) Matthew Dolan mdolan@ryerson.ca
Course Evaluation	(The following is a Table and you can add/remove rows/columns as needed) Midterm Exam 30 % Lab Projects 30 % Final Exam 40 % **TOTAL**: 100 %
Examinations	1.5 hour midterm exam with date to be determined in class. Final exam, during exam period, 3 hours, closed-book covering all course materials.
Other Evaluation and/or Information	None

Course Contents

Chap.	Sections	hours	Topic, description
1	N/A	6	**Module 1 - Modeling of wire channels** 1) Resistance, capacitance, and inductance of wire channels 2) Lumped models of wire channels 3) Distributed models of wire channels 4) Transmission-line models of wire channels
2	N/A	3	**Module 2 - Electrical signaling** 1) Single-ended signaling 2) Fully differential signaling 3) Pseudo-differential signaling 4) Low-voltage differential signaling (LVDS) 5) Voltage-mode signaling versus current-mode signaling Incremental signaling
3	N/A	3	**Module 3 - Fundamentals of serial links**

			1) Pulse amplitude modulation (PAM) 2) Pulse width modulation (PWM) 3) Eye diagrams 4) Inter-symbol interference (ISI) 5) Bit-error rate 6) Test of serial links
4	N/A	9	**Module 4 – Phase/Frequency-locked loops (PLLs/FLLs)** 1) Phase-frequency detectors 2) Charge pumps 3) Ring oscillators 4) Stability of PLLs 5) Phase noise of PLLs 6) Introduction of all-digital PLLs
5	N/A	9	**Module 5 - Channel equalization** 1) Bandwidth enhancement techniques 2) Pre-emphasis 3) Continuous-time linear equalization (CTLE) 4) Decision feedback equalization (DFE) 5) Adaptive DFE
6	N/A	6	**Module 6 - Clock and data recovery (CDR)** 1) Phase-picking CDR Phase-tracking CDR

Laboratory/Tutorials

Week	Title	Room
2-3	Laboratory Design Project 1 : Wire channels	ENG 412
4-5	Laboratory Design Project 2 : Continuous-time linear equalizers	ENG 412
6-7	Laboratory Design Project 3 : Phase-locked loops	ENG 412
8-9	Laboratory Design Project 4 : Pre-emphasis	ENG 412
10-11	Laboratory Design Project 5 : Decision feedback equalizers	ENG 412
12-13	Laboratory Design Project 6 : Clock and data recovery	ENG 412

Important Notes

1. All of the required course-specific written reports will be assessed not only on their technical/academic merit, but also on the communication skills exhibited through these reports.

2. All assignment and lab/tutorial reports must have the standard cover page which must be signed by the student(s) prior to submission of the work. Submissions without the cover page **will not** be accepted. The cover page can be found on the departmental web site: Standard Assignment/Lab Cover Page

3. Should a student miss a mid-term test or equivalent (e.g. studio or presentation), with appropriate documentation, a make-up assessment ***may*** be scheduled. Alternatively, the weight of the missed work is placed on the final exam, or another single assessment. This may not cause that exam or assessment to be worth more than 70% of the student's final grade. If a student misses a scheduled make-up test or exam, the grade may be distributed over other course assessments even if that makes the grade on the final exam worth more than 70% of the final grade in the course. Make-up assessments cover the same material as the original assessment but need not be of an identical format.

4. Students who miss a final exam for a verifiable reason and who cannot be given a make-up exam prior to the submission of final course grades, must be given a grade of INC (as outlined in the *Grading Promotion and Academic Standing Policy)* and a make-up exam (normally within 2 weeks of the beginning of the next semester) that carries the same weight and measures the same knowledge, must be scheduled.

5. Medical or Compassionate documents for the missing of an exam must be submitted within 3 working days of the exam. Students are responsible for notifying the instructor that they will be missing an exam as soon as possible.

6. **If a student is requesting accommodation due to a religious, aboriginal and/or spiritual observance, he or she must submit a Request for Accommodation of Student Religious, Aboriginal, and Spiritual Observance AND an Academic Consideration form within the FIRST TWO WEEKS OF CLASS or, for a final examination, within two weeks of the posting of the examination schedule**. If the required absence occurs within the first two weeks of classes, or the dates are not known well in advance as they are linked to other conditions, these forms should be submitted with as much lead time as possible in advance of the required absence.
   Both documents are available at http://www.ryerson.ca/senate/forms/relobservforminstr.pdf. Full-time or part-time degree students must submit the forms to their own program department or school.

7. The results of the first test or mid-term exam will be returned to students before the deadline to drop an undergraduate course in good Academic Standing.

8. Students are required to adhere to all relevant University policies including:
   - Undergraduate Grading, Promotion and Academic Standing: http://www.ryerson.ca/senate/policies/pol46.pdf
   - Student Code of Academic Conduct: http://www.ryerson.ca/senate/policies/pol60.pdf
   - Student Code of Non-Academic Conduct: http://www.ryerson.ca/senate/policies/pol61.pdf
   - Undergraduate Academic Consideration and Appeals: http://www.ryerson.ca/senate/policies/pol134.pdf
   - Examination Policy: http://www.ryerson.ca/senate/policies/pol135.pdf
   - Course Management Policy: http://www.ryerson.ca/senate/policies/pol145.pdf
   - Accommodation of Student Religious, Aboriginal and Spiritual Observance: http://www.ryerson.ca/senate/policies/pol150.pdf
   - Establishment of Student E-mail Accounts for Official University Communication: http://www.ryerson.ca/senate/policies/pol157.pdf

9. Students are required to obtain and maintain a Ryerson e-mail account for timely communications between the instructor and the students.

10. Any changes in the course outline, test dates, marking or evaluation will be discussed in class prior to being implemented.

11. Assignments, projects, reports and other deadline-bound course assessment components handed in past the due date will receive a mark of ZERO. Marking information will be made available at the time when such course assessment components are announced.

12. If you have taken the course previously and are currently looking to get a laboratory exemption, then you must fill out this form: http://www.ee.ryerson.ca/guides/ECE-LabExemptionForm.pdf

Approved by: _____ Date _____
Course Instructor

Approved by: _____ Date _____
Associate Chair or Program Director