COE608: Computer Org. and Architecture

Final Examination

General Instructions **Maximum Marks: 75**

a) Total time allowed is **2 hours**.
b) The examination has **2** sheets and **5** questions. Answer all the questions.
c) Some questions contain special instructions. Please ensure that you read them carefully.
d) All questions are not of the same difficulty and value. Consider this when allocating time for their solution.
e) If a question proves to be too hard for you to solve, go on to another question! Return to the troublesome question when time permits.
f) Estimated time for each question is equivalent to the marks assigned to it.

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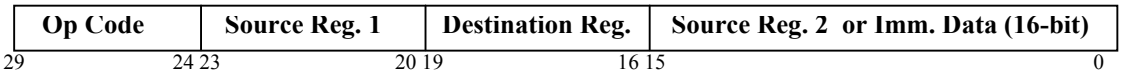
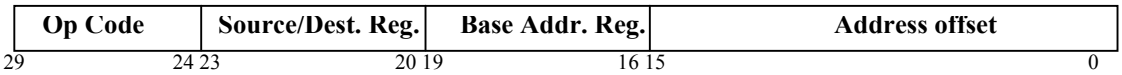
1. Consider a RISC processor to be developed having three instruction formats as given below.

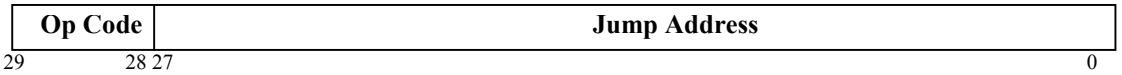
a. Register-Register instructions (R- type)



b. Load-Store instructions (LS –type)



c. Jump instructions (J-type)



Determine the following parameters of the computer hardware to be designed.

i) Total number of instructions that can be implemented in the processor (including R, LS and J-type).
ii) Size of the register file.
iii) Assuming that a program can access data from any place in the Main memory, determine the maximum size of the main Memory in Mbytes.

MARKS: (2+2+2)

2. Suppose we are considering a change to the instruction set of processor architecture. The base machine initially has only loads and stores to memory, and all operations work on the registers. Measurements of the load-store machine for the application showing the instruction mix and clock cycle counts per instruction are given below.

Instruction type	Instruction Frequency	Clock cycle count
ALU ops	40%	2
Loads	30%	3
Stores	10%	3
Branches	20%	2

Let's assume that 25% of the arithmetic logic unit (ALU) operations directly use a loaded operand that is not used again. We propose adding ALU instructions that have one source operand in memory e.g. a new add instruction "`addm $s1,100($s2)`" is equivalent to "`$s1 <= $s1 + Memory[$s2+100]`". These new register-memory instructions have a clock cycle count of 3. Assume that the extended instruction set does not affect the clock cycle time of the modified machine and every register memory instruction used in the application replaces a pair of ALU ops and Load instructions.

i) Calculate the CPI of the base machine as well as the extended instruction set machine.
ii) Would this change to the instruction set improve the performance? Justify your answer.

MARKS: (10+8)

Please turn over for Question No. 3

3. i) Convert the decimal digits $(-2434)_{10}$ and $(-1346)_{10}$ into 16-bit 2's complement binary format.
   ii) Subtract $(-1346)_{10}$ from $(-2434)_{10}$ i.e. $[(-2434)_{10} - (-1346)_{10}]$ using 2'complement arithmetic and determine the magnitude of the result in binary form.
   iii) Write a VHDL ENTITY for a 4-to-1 multiplexor with 2-bit inputs and a 2-bit output.

MARKS: (4+4+3)

4. Design a digital system that multiplies two 8-bit unsigned binary numbers by repeated addition method. For instance, to multiply 7 by 3, the digital system adds the multiplicand three times: 7 + 7 + 7 = 21.
   Let the multiplicand be in register BR, the multiplier in register AR, and the product in register PR. A full-adder circuit adds the contents of BR to PR and stores the result in PR. A zero detection circuit Z checks the contents of AR when it becomes zero after each time it is decremented.
   i) Design an optimal datapath of the circuit showing the size and control signals for each hardware component (e.g. Registers, Adder, etc.).
   ii) Develop an ASM chart for the system control unit with minimum number of state boxes.

MARKS: (10+10)

5. Consider a RISC pipelined processor with separate instruction and data memory and having three instruction formats; R, LS and J types with the following stages:
   - R-type: IF, ID/RA, ALU and WB;
   - LS-type (Load and Store): IF, ID/RA, ALU(MAddr), MA and WB;
   - J-type: IF, ID/RA, ALU

   where: IF = Instruction Fetch, ID/RA = Instruction Decode and Register Access
   ALU = ALU operation, ALU(MAddr) = Memory Address Calculation by the ALU
   MA = Memory Access (read or write), WB = Write Back

   Each stage requires one clock cycle and following instruction sequence is executed:

```
add  $s2,$s1,$s3
and  $s6,$s2,$s5
lw   $s4, 1004($s7)
or   $s7,$s4,$s2
sw   $t7,1008($s4)
```

   i) List the dependencies that will cause stalls for the above instruction sequence and identify the types of hazards that will appear due to these dependencies.
   ii) With the help of a pipeline-timing chart, calculate the total number of clock cycles needed to execute the above sequence on a pipelined CPU that does not have any forwarding hardware.
   iii) Identify those stalls that can be overcome by a forwarding hardware facility.
   iv) What difference would it make to the type of hazards and forwarding requirements if the first instruction in the sequence is replaced by a load instruction given next? `lw $s2,1000($zero)`

MARKS: (5+5+5+5)