Introduction to System-on-Chip

COE838/EE8221 Systems-on-Chip Design
http://www.ee.ryerson.ca/~courses/COE838/

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Electrical and Computer Engineering
Ryerson University

Overview

• Course Management
• Introduction to SoC
• SoC Applications
• On-Chip Interconnections
• Bus-based and NoC based SoC Interconnects

Introductory Articles on SoC available at the course webpage
COE838/EE8221: Systems-on-Chip Design

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Consultation Hours: Thursday 12:30-2:00PM or by Appointment

Department of Electrical and Computer Engineering
Ryerson University
Lectures, Labs and Projects

Half Notes
- Students need to take notes and also require text-reference books and some research articles identified by the instructor.

Labs and Project
- Aimed at concept reinforcement and practical experience.

Assessment and Evaluation
- Labs: 15%
- Project: 15%
- Midterm Exam: 25% (Thursday: February 14, 2019 during lecture hours in DSQ 03 Theatre)
- Final Exam: 45%

Lectures, Labs, Projects and other support material will be available at the course website:
http://www.ee.ryerson.ca/~courses/coe838/
Course Text/Reference Books and other Material

Text and Other Books


Some Articles, Embedded Processors and other Data Sheets are available at the Course Website:  http://www.ee.ryerson.ca/~courses/coe838/
Main Lecture Topics

1. Introduction to System on Chip (SoC)
   * An SoC Design Approach
2. SystemC and SoC Design:
   * Co-Specification, System Partitioning, Co-simulation, and Co-synthesis
   * SystemC for Co-specification and Co-simulation
3. Hardware-Software Co-Synthesis, Accelerators based SoC Design
4. Basics of Chips and SoC ICs:
   * Cycle Time, Die Area-and-Cost, Power,
   * Area-time-Power Tradeoffs and Chip Reliability
5. System-on-Chip and SoPC (System on Programmable Chips)
6. SoC CPU/IP Cores
   * ARM Cortex A9, NIOS-II, OpenRISC, Leon4 and OpenSPARC
7. SoC Interconnection Structures: Bus-based Interconnection
   * AMBA Bus, IBM Core Connect, Avalon, Interconnection Structures
8. Network on Chip - NoC Interconnection and NoC Systems
9. Multi-core and MPSoC Architectures
10. SoC Application Case Studies (time permitting)
System on a Chip

- An IC that integrates multiple components of a system onto a single chip.
- MPSoC addresses performance requirements.
Samsung S3C6410 Platform

- System Peripheral
  - RTC
  - PLL x 3
  - Timer w/ PWM 4ch
  - Watch Dog Timer
  - DMA(32ch)
  - Keypad (8 x 8)

- Connectivity
  - GPIO
  - I2S 24-bit D-5.1ch
  - AC97 & PCM
  - 2ch I2C
  - 4ch UART & IrDA v1.1
  - 8ch 12bit ADC
  - 2ch HS-SPI
  - HSI & Modem I/F: 8KB DPRAM
  - USB OTG 2.0
  - USB Host 1.1
  - SDHC/HS-MMC

- ARM Core
  - ARM 1176JZF-S
  - I / D cache 16KB/16KB
  - I / D TCM 16KB/16KB
  - 533MHz @1.1V
  - 667MHz @1.2V
  - 800MHz @TBD

- Multimedia Acceleration
  - Camera controller: 4MP
  - Multi Format CODEC (H.264 / MPEG4/ VC1)
  - NTSC, PAL TV out (+ Image Enhancement)
  - JPEG codec
  - 2D Graphics
  - 3D Graphics :9M tri/sec (OpenGL ES 1.1/2.0)
  - Standalone Rotator and post processor

- Memory Subsystem
  - SRAM/ROM/NOR/ OneNAND
  - Mobile SDRAM
  - DDR & SDRAM
  - NAND Flash / 8-bit ECC, 4KB page mode
  - CF 3.0 / ATA controller

- Secure Boot ROM
- Crypto Engine
- X64/32 Multi-layer AXI/AHB Bus
- Power Management
- TFT LCD Controller
  - 24/18bit or 8bit for Dual i80
  - 1024x1024 output
  - 5-layer PIP
  - 16bit a-blending

Introduction to SoC Design
S3C6410 System-on-Chip

• A 16/32-bit RISC low power, high performance micro-processor
• Applications include mobile phones, Portable Navigation Devices and other general applications.
• Provide optimized H/W performance for the 2.5G and 3G communication services,
• Includes many powerful hardware accelerators for motion video processing, display control and scaling. An
• Integrated Multi Format Codec (MFC) supports encoding and decoding of MPEG4/H.263, H.264.
• Many hardware peripherals such as camera interface, TFT 24-bit LCD controller, power management, etc.
S3C6410 based Mobile Processor

Navigation System

iPhone based on ARM1176JZ

S3C6410
Samsung S5PC100 SoC used in iPhone 3GS
S5PC100 Samsung SoC

S5PC100 has various functionalities:

- Wireless communication, Personal navigation, Camera
- Portable gaming, Video player and Mobile TV into one device.
- S5PC100 has a 32-bit ARM Cortex A8 RISC microprocessor that operates up to 833MHz.
- 64/32-bit internal bus architecture
- Used in iPhone 3GS and iPod touch 3rd generation.
Moore’s Law

…the performance of an IC, including the number components on it, doubles every 18-24 months with the same chip price … - Moore - 1960
# Technology Past Roadmap

<table>
<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>Technology</td>
<td>180nm</td>
<td>130nm</td>
<td>100nm</td>
<td>70nm</td>
<td>50nm</td>
<td>35nm</td>
</tr>
<tr>
<td>DRAM/introduction</td>
<td>1G</td>
<td>2~4G</td>
<td>8G</td>
<td>-</td>
<td>64G</td>
<td>-</td>
</tr>
<tr>
<td>Transistors/chip (µP) (M)</td>
<td>110</td>
<td>220~441</td>
<td>882</td>
<td>2,494</td>
<td>7,053</td>
<td>19,949</td>
</tr>
<tr>
<td>Chip size (µP) (mm³)</td>
<td>450</td>
<td>450~567</td>
<td>622</td>
<td>713</td>
<td>817</td>
<td>937</td>
</tr>
<tr>
<td>Number of signal I/O (µP)</td>
<td>768</td>
<td>1,024</td>
<td>1,024</td>
<td>1,280</td>
<td>1,408</td>
<td>1,472</td>
</tr>
<tr>
<td>Power/Ground I/O (µP)</td>
<td>1,536</td>
<td>2,018</td>
<td>2,018</td>
<td>2,560</td>
<td>2,816</td>
<td>2,944</td>
</tr>
<tr>
<td>On-chip local clock (MHz) (high performance)</td>
<td>1,250</td>
<td>2,100</td>
<td>3,500</td>
<td>6,000</td>
<td>10,000</td>
<td>13,500</td>
</tr>
<tr>
<td>On-chip across-chip clock (MHz) (high performance)</td>
<td>1,200</td>
<td>1,600</td>
<td>2,000</td>
<td>2,500</td>
<td>3,000</td>
<td>3,600</td>
</tr>
<tr>
<td>Off-chip speed (MHz) (high perf., peripheral buses)</td>
<td>480</td>
<td>885</td>
<td>1,035</td>
<td>1,285</td>
<td>1,540</td>
<td>1,800</td>
</tr>
<tr>
<td>Power (W) H.P./H.H.</td>
<td>90/1.4</td>
<td>130/2.0</td>
<td>160/2.4</td>
<td>170/2.0</td>
<td>174/2.2</td>
<td>183/2.4</td>
</tr>
<tr>
<td>Power supply (V) H.P./H.H.</td>
<td>1.8/1.5</td>
<td>1.5/1.2</td>
<td>1.2/0.9</td>
<td>0.9/0.6</td>
<td>0.6/0.5</td>
<td>0.6/0.3</td>
</tr>
<tr>
<td>Metal levels # (µP/SoC)</td>
<td>7/6</td>
<td>8/7</td>
<td>9/8</td>
<td>9/9</td>
<td>10/10</td>
<td>10/10</td>
</tr>
</tbody>
</table>

H.P: High performance µP - MicroProcessor
H.H: Hand Held Devices
Evolution: Boards to SoC

Evolution:
- IP based design
- Platform-based design

Some Challenges
- HW/SW Co-design
- Integration of analog (RF) IPs
- Mixed Design
- Productivity

Emerging new technologies
- Greater complexity
- Increased performance
- Higher density
- Lower power dissipation
What is System-on-Chip

SoC: More of a System not a Chip

* In addition to IC, SoC consists of software and interconnection structure for integration.

SoC may consists of all or some of the following:

- Processor/CPU cores
- On-chip interconnection (busses, network, etc.)
- Analog circuits
- Accelerators or application specific hardware modules
- ASICs Logics
- Software – OS, Application, etc.
- Firmware
System on a Chip

On-Chip Components?

A processor or multiple processors

* Including DSPs, microprocessors, microcontrollers

Cores (IPs): On-chip memory, accelerators, peripherals (i.e. USB, ETH, etc.), PLLs, power management, etc.
ASIC to System-on-Chip

**ASICs:** Application Specific ICs are close to SoC designed to perform a specific function for embedded and other applications.

* ASIC vendors supply libraries for each technology they provide. Mostly, these libraries contain pre-designed/verified logic circuits.

* SOC is an IC designed by combining multiple stand-alone VLSI designs to provide a functional IC for an application. It composes of pre-designed models of complex functions e.g. cores (IP block, virtual components, etc.) that serve various embedded applications.
ASIC Design Flow

Long Time to Design

DVT: Design, Verification and Testing

Top Level Design
Unit Block Design
Unit Block Verification
Integration and Synthesis
Trial Netlists
Timing Convergence & Verification
System Level Verification
Fabrication
DVT Prep
DVT Prep

Time in Weeks

5 10 10 4 13 ?? 4 6

Time to Mask order

42 52

Introduction to SoC Design
System-on-Chip Design Flow

• Specify: What does the customer really want?

• Architect:
  * Find the most cost and performance effective architecture to implement it?
  * Which existing components can we adapt & re-use?

• Evaluate: What is the performance impact of a cheaper architecture?

• Implement: What can we generate automatically from libraries and customization?
  Use separate computation, communication, etc.
Due to Chip Complexity and lower IC area, it is difficult to reduce Placement, Layout and Fabrication steps time.

There is need to reduce the time of other steps before Placement, Layout and Fabrication steps.

One should consider Chip Layout issues up-front.

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Introduction to SoC Design
System-on-Chip

- CPU
- DSP
- MPEG CORE
- VGA CORE
- Analog ADC/DAC
- Other Component
Introduction to SoC Design

SOC Structure

A tile of the chip

A computational block

A communication link
SOC: System on Chip

- SOC cannot be considered as a large ASIC
  - Architectural approach involving significant design reuse
  - Addresses the cost and time-to-market problems
- SOC design is significantly more complex
  - Need cross-domain optimizations
  - IP reuse will increase productivity, but not enough
  - Even with extensive IP reuse, many of the ASICs design problems will remain, and more …
SOC Applications

● SOC Design include embedded processor cores, and a significant software component, which leads to additional design challenges.
● An SOC is a system on an IC that integrates software and hardware Intellectual Property (IP) using more than one design methodology.
● The designed system on a chip is application specific.

Typical applications of SOC:

- Consumer devices.
- Networking and communication.
- Biomedical Devices.
- Other segments of electronics industry.

Microprocessor, Media processor, GPS controllers, Cellular/Smart phones, ASICs, HDTV, Game Consoles, PC-on-a-chip
IP: Intellectual Property Cores

IP cores can be classified into three types:

**Hard IP** cores are hard layouts using physical design libraries. The integration of hard IP cores is simple and easy. However, they are technology dependent and lack flexibility.

**Soft IP** cores are generally in VHDL/Verilog code providing functional descriptions of IPs. These cores are flexible and reconfigurable. However, these soft IP cores must be synthesized and verified by the user before integrating them.

**Firm IP** cores provide the advantage of both balancing the high performance and optimization properties of hard IPs along with the flexibility of soft IPs. These cores are provided in the form of netlists to specific physical libraries after synthesis.
## Some IP Examples

<table>
<thead>
<tr>
<th>Category</th>
<th>Intellectual Property</th>
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</thead>
<tbody>
<tr>
<td>Processor</td>
<td>ARM7, ARM9, and ARM10, ARC</td>
</tr>
<tr>
<td>Application-Specific DSP</td>
<td>ADPCM, CELP, MPEG-2, MPEG-4, Turbo Code, Viterbi, Reed Solomon, AES</td>
</tr>
<tr>
<td>Mixed Signal</td>
<td>ADCs, DACs, Audio Codecs, PLLs, OpAmps, Analog MUX</td>
</tr>
<tr>
<td>I/Os</td>
<td>PCI, USB, 1394, 1284, E-IDE, IRDA</td>
</tr>
<tr>
<td>Miscellaneous</td>
<td>UARTs, DRAM Controller, Timers, Interrupt Controller, DMA Controller, SDRAM Controller,</td>
</tr>
<tr>
<td></td>
<td>Flash Controller, Ethernet 10/100 MAC</td>
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</tbody>
</table>
Multi-Core (Processor) System-on-Chip

Inter-node communication between CPU/cores can be performed by message passing or shared memory. Number of processors in the same chip-die increases at each node (CMP and MPSoC).

• Memory sharing will require: **Shared Bus**
  * Large Multiplexers
  * Cache coherence
  * Not Scalable

• Message Passing: **NOC: Network-on-Chip**
  * Scalable
  * Require data transfer transactions
  * Overhead of extra communication
Buses to Networks

• Architectural paradigm shift: Replace wire spaghetti by network
• Usage paradigm shift: Pack everything in packets
• Organizational paradigm shift
  ▪ Confiscate communications from logic designers
  ▪ Create a new discipline, a new infrastructure responsibility
MPSoC

MPSoC is a system-on-chip and it contains multiple instruction-set processors (CPUs).

- A typical MPSoC is a heterogeneous multiprocessor where several different types of processing elements (PEs).
- The memory system may also be heterogeneously distributed around the machine, and the interconnection structure between the PEs and the memory may also be heterogeneous.
- MPSoCs often have large memory. The application device can have embedded memory on-chip, and may rely on off-chip commodity memory.
SOC: System on Chip

Several CPUs are now actually considered as SoCs!

- CPUs now contain the CPU itself, along with integrated graphics processors, PCI express, memory controllers etc. all on a single die

Advantages?
Disadvantages?

iPad3’s CPU SoC Circuit → A5

PC Motherboard – CPU with support ICs
Exynos 5410 Octa Processor SoC

Octa core CPU, big.LITTLE processing
3D graphics – fast/efficient operation for smartphone/tablets.
12.8 GB/s memory bandwidth, 1080p 60 fps video.
Where are we heading?

- Introduction to System on Chip - An SoC Design Approach.
- SystemC for SoC Design: Co-Specification and Simulation.
- Hardware-Software Co-synthesis and Accelerator based SoCs.
- Basics of Chips and SoC ICs.
- Hardware-Software Co-synthesis and Accelerator based SoCs.
- SoC CPU/IP Cores: ARM Cortex A9.
- SoC Interconnection Structures: Bus-based Interconnection.
- NoC: Network on Chip.
- Multi-core and MPSoC (Multiprocessor SoC) Architectures.
- SoC Case Studies (if time permits).
3D transistor reduces the chip size while increasing performance and energy efficiency.

2D Transistor

3D Transistor

Number of roads electrons travel

1-way \rightarrow 3-way

Shorter travel distance

2D \rightarrow 3D