PACKAGING

IC Packaging

- Purposes
  1) Electrical connections
     - Signals
     - Power and ground
  2) Aids heat dissipation
     - Increase effective surface area for increased convection
     - Heat conduction into PC board
  3) Physical protection for IC
     - e.g., against breakage
  4) Environmental protection
     - Hermetic (airtight) seal
     - e.g., against corrosion or moisture
Rent’s Rule

- Empirical formula
- \( P = K G^\beta \)
- \( P \) = number of input/output connections (pins)
- \( K \) = average number of I/Os per “gate”
- \( G \) = number of “gates”
- \( \beta \) = empirically-found parameter that varies according to application; generally between 0.1 and 0.7

| Package Metrics |
|-----------------|-----------|
| **Electrical**   |           |
| - Low capacitance    |         |
| - Low inductance     |         |
| - Low resistance     |         |
| **Mechanical**      |           |
| - Reliable across temperature variations (thermal expansion matching) | |
| **Thermal**         |           |
| - Low thermal resistance to get the heat out | |
| **Economical (cost)** |       |
| - Purchase of package |  |
| - Assembly (chip and board assembly) |  |
| - System (heat removal equipment included) |  |
Package Materials

- Plastic
  - Low cost
  - Typically requires a custom-designed package
- Ceramic
  - Better heat transfer characteristics
  - Generally more reliable
  - More likely an off-the-shelf part can be used
    - Good for research and prototyping

Interconnection Levels

- Multiple levels of packaging
  - Ease of handling
  - Reuse of intermediate-sized modules (e.g., DRAM memory stick)
    - Use in multiple products
    - Upgradeable in field
    - Repairable in field
Solder

- Solder is the universal electrical “glue”
  - tin and lead alloy: 50/50%, 63/37% Sn/Pb eutectic mixture
  - low melting temperature: 183 °C or 361.4 °F for eutectic
  - good electrical conductivity
- Large efforts now under way to eliminate or reduce the use of lead
  - RoHS - Restriction of Hazardous Substances Directive
  - Many replacements available
    - Typical ones use Tin, Silver, Copper; maybe Bismuth, Indium, Zinc, Antimony

PC Board

Source: J-Machine, Dally
System

- J-Machine
- Built at MIT and Stanford in the early 1990’s
- 1024 processors

IBM Blue Gene/L

- The fastest supercomputer in the world is a 131,072-processor Blue Gene machine
IBM Blue Gene/L

- **BlueGene/L**: 1/100th the physical size (320 vs 32,500 square feet) consumes 1/28th the power (216KW vs 6,000KW) - compared to Earth Simulator

- Attained a sustained performance of **70.72 Teraflops**
  - eclipsing 3 year old top mark of **35.86 Teraflops** - Japanese Earth Simulator
  - recent mark of **42.7 Teraflops** at the NASA's Ames research center

**Chip to Package Connections**

1) Wire bonding
   - die attached
   - gold or aluminum wires
   - one at a time
   - not entirely repeatable
   - Electrical characteristics:
     - R: low
     - C: low
     - L: ~1 nH/mm
Bonding Techniques

Wire Bonding

Wire Bonds

- Optical microscope view of bond wires for a two-pad package
Wire Bonds

- SEM view of bond wires for a two-pad package

Source: Assurance Technology

Wire Bonds

- SEM view of a single bond wire attachment

Source: Assurance Technology
Wire Bonds

- Gold wire bond on aluminum die pad

Source: SEM Lab, Inc.

Wire Bonding Machine

- Wire bonding machine

Source: TWI, Ltd.
Chip to Package Connections

2) Tape automated bonding (TAB)
   - Die attached to metal lead frame printed on polymer film using solder bumps
   - Tape then connected to package
   - Fast and parallel operation
   - Lower electrical parasitics (R, L, C)

Tape-Automated Bonding (TAB)

(a) Polymer Tape with imprinted wiring pattern.
(b) Die attachment using solder bumps.

Source: Digital Integrated Circuits, 2nd ©
Tape-Automated Bonding (TAB)

Chip to Package Connections

3) Flip chip solder bump
   - chip placed face down in package
   - connected with solder bumps
   - very low parasitics
   - allows “area pads”
     • pads can cover chip area and are not limited to chip periphery
Flip-Chip Bonding

Package to Board Connections
1) Through Hole

- Classic approach
- Holes drilled and plated with copper
- Soldering
  - Chips placed inside holes
  - Bottom of board passed through a molten solder “wave”
Package to Board Connections
2) Surface Mount Technology (SMT)

- More wiring room inside PC board
- Reduced space between package leads
- Chips on both sides of board
- Stronger PC board
- Soldering
  - Solder paste applied
  - Heat supplied by intense infrared light, heated air,…

Package-to-Board Interconnect

(a) Through-Hole Mounting  
(b) Surface Mount

Source: Digital Integrated Circuits, 2nd ©
SMT Leads

a) Gull-wing SMT package leads
   - Soldering issues

Ex: Thin Small Outline Package Type II (TSOP Type II)

b) J-Lead SMT package leads
   - Many package types available
   - Less board space than gull wing

Ex: Small Outline J-lead (SOJ)
SMT “leads”

c) Solder Balls
   - Similar to flip chip but at package-to-board level
   - Very low parasitics
   - Example BGA solder ball
     (with highlighted crack)

Package Examples

Through hole
Surface mount

Source: Digital Integrated Circuits, 2nd ©
Package Types
DIP – Dual In-Line Package

- One of the oldest packaging technologies
- Low performance
- 48-64 pin packages are huge
- Cheap and abundant
- Plastic and ceramic

http://www.mameworld.net/gurudumps/MyStuff/packages.html
http://www.tms.org/pubs/journals/JOM/9903/Frear-9903.html
http://www.aqueclopelpae.com/packaging.html
http://www.arlabs.com/help.htm

Package Types
ZIP – Zig-Zag In-Line Package

- Not very common

http://www.mameworld.net/gurudumps/MyStuff/packages.html
Package Types
SOP – Small Outline Package

• SOP includes a large family of packages
  – SOIC – Small Outline Integrated Circuit
  – SSOP – Shrink Small Outline Package
  – QSOP – Quarter-size Small Outline Package
  – TSSOP – Thin Shrink Small Outline Package
  – MSOP – Mini Small Outline Package

http://www.carsem.com/services/package.php
http://www.mameworld.net/gurudumps/MyStuff/packages.html

Package Types
TSOP – Thin Small Outline Package

• One of the smallest packages available
• Type I – leads on short sides

• Type II – leads on long sides

http://www.mameworld.net/gurudumps/MyStuff/packages.html
Package Types

QFP – Quad Flat Package

- Common in modern electronics

- TQFP – Thin Quad Flat Package
  - Typical thickness 1.4 mm

Package Types

SOJ – Small Outline J-lead

- “J” leads on two sides

http://www.mameworld.net/gurudumps/MyStuff/packages.html
http://www.asetwn.com.tw/content/2-1-2.html
http://www.toshiba.co.jp/indexen/pat/tp-disclosure/p258717.htm
Package Types
PLCC – Plastic Leaded Chip Carrier

- Also called QFJ – Quad Flat J-lead
- Common in many products

PGA – Pin Grid Array Package

- Material—the main body consists of co-firing multilayer alumina ceramics, and pin terminals made of an alloy of iron, nickel, and cobalt are attached with silver-brazing to the main body.
- 400+ pins possible
- Cavity up
- Cavity down
Package Types
BGA – Ball Grid Array

- Very common for high-volume high-pin-count chips
  - 200-500 I/Os is common
  - Excellent electrical characteristics
  - Good heat conduction into PC board
  - Difficult to inspect once soldered to PC board
  - Difficult to replace

![BGA with Flip-Chip](image)

Package Parameters

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Capacitance (pF)</th>
<th>Inductance (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>68 Pin Plastic DIP</td>
<td>4</td>
<td>55</td>
</tr>
<tr>
<td>68 Pin Ceramic DIP</td>
<td>7</td>
<td>20</td>
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<tr>
<td>256 Pin Pin Grid Array</td>
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<td>15</td>
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<tr>
<td>Wire Bond</td>
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<td>1</td>
</tr>
<tr>
<td>Solder Bump</td>
<td>0.5</td>
<td>0.1</td>
</tr>
</tbody>
</table>

Typical Capacitances and Inductances of Various Package and Bonding Styles (from [Sze83])

Source: Digital Integrated Circuits, 2nd
Mounting Die Directly to a Substrate

A. Multi-chip Module
   - silicon on silicon
   - many of other ceramic materials used
   - testing is big issue (“known good die”)
B. “Chips on Board”
C. System in Package (SiP)

Multi-Chip Module

Source: Digital Integrated Circuits, 2nd ©
Package Types
SiP – System in Package

- Increasingly popular for high-volume small form factor products
- Can combine wire bonds with flip chip
- Nice solution for an application system with different types of chips and “passives” (R, L, C)

http://www.carsem.com/services/package.php