1. Objectives

This course is designed to offer an introduction in the theory and engineering design principles of the modern Reconfigurable Computing Systems (RCS) – one of the most rapidly growing sectors of the high-performance computer technology. The emphasis is in understanding of the concepts of architecture reconfigurability, programmable logic devices and optimization of the RCS architecture to the task algorithm and data structure. The course covers basics of the Complex Programmable Logic Devices (CPLD) and Field Programmable Gate Array (FPGA) organization and RCS architectures based on these devices. The survey of RCS and areas of their application also is provided. Languages and Compilers for the RSC are other aspects to be covered in this course. Course gives brief description of RCS application in DSP, Video / Image Processing and Supercomputing applications. Then the specifics of RCS design will be discussed including DSP and Embedded processors design flow, modular and incremental design. Synthesis, simulation and verification design tools also will be discussed in details.

2. Course Outline

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<tr>
<th>WEEK</th>
<th>LECTURE</th>
<th>PROJECT</th>
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<tbody>
<tr>
<td>1</td>
<td>Introduction: Course content &amp; organization, Definition of RCS: Reconfigurable Computing Systems and RCS classification. Component basis of the RCS: Complex Programmable Logic Devices (CPLD) and Field Programmable Gate Array (FPGA)</td>
<td>Announcement of projects, project format and report organization. Selection of project topic</td>
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<td>2</td>
<td>RCS Architectures: Fine-grain and Coarse-grain architectures. RCS-supercomputers, Massively parallel FPGA array, Data-stream processing RCS, Hybrid RCS architectures Languages and Compilers for RCS: Algorithmic languages for RCS, Hardware Description Languages (HDL). High-level of Compilation and low-level design flow</td>
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### WEEK 4
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<td><strong>RCS Development</strong>&lt;br&gt;Architectural synthesis stage: High-level synthesis and multi-parametric optimization.</td>
<td>Analysis of the state-of-the-art in selected area of research.</td>
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<td><strong>RCS Development</strong>&lt;br&gt;Architecture-to-hardware implementation: Schematic and HDL based design flows</td>
<td>Classification and Summary</td>
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### WEEK 5
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<td><strong>RCS implementation</strong>&lt;br&gt;DSP and Embedded Processor-based design flows. Modular and Incremental design.</td>
<td>Preparation of the Project report according to requested format</td>
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<td><strong>RCS implementation</strong>&lt;br&gt;Intellectual Property cores. Concept of Virtual Hardware Component (VHC) and Application Specific Virtual Processor (ASVP). Spatial and temporal partitioning of FPGA resources.</td>
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### WEEK 6
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<td><strong>RCS verification and debugging</strong>&lt;br&gt;Synthesis, Simulation and Verification tools. Virtual instruments &amp; performance analyzers.</td>
<td>Project report submission</td>
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<td><strong>Course review</strong></td>
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### WEEK 7
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<th>LECTURE</th>
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<td><strong>Final Examination</strong></td>
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### 3. Course Prerequisites
1. Computer Organization and Architecture courses (similar to COE608 and COE818)
2. Digital Systems Engineering (similar to COE758)

### 4. Course Text

### 5. Marking Scheme
- Project = 45%
- Final Exam = 55%

All of the required course specific written reports will be assigned not only on their technical or academic merit, but also on the communication skills of the author as exhibited through these reports.

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